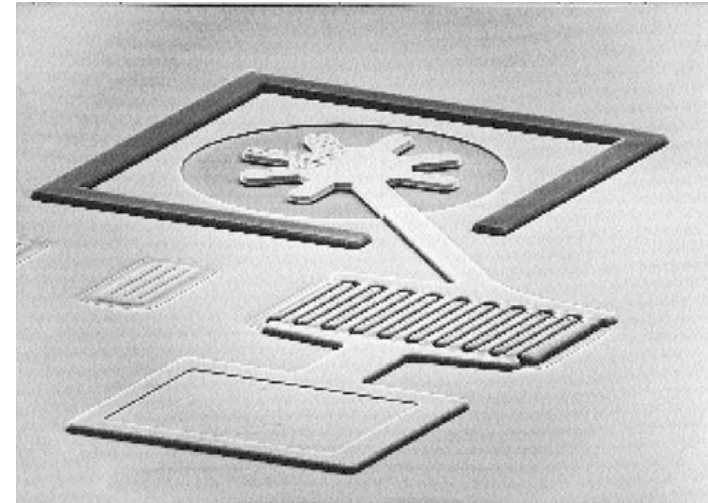
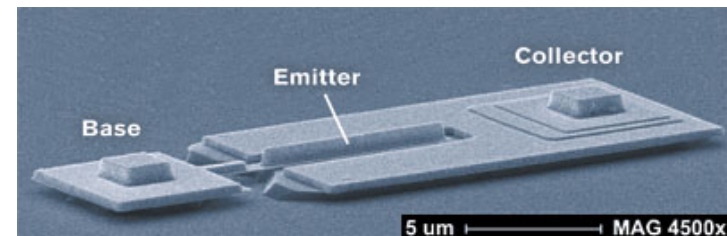


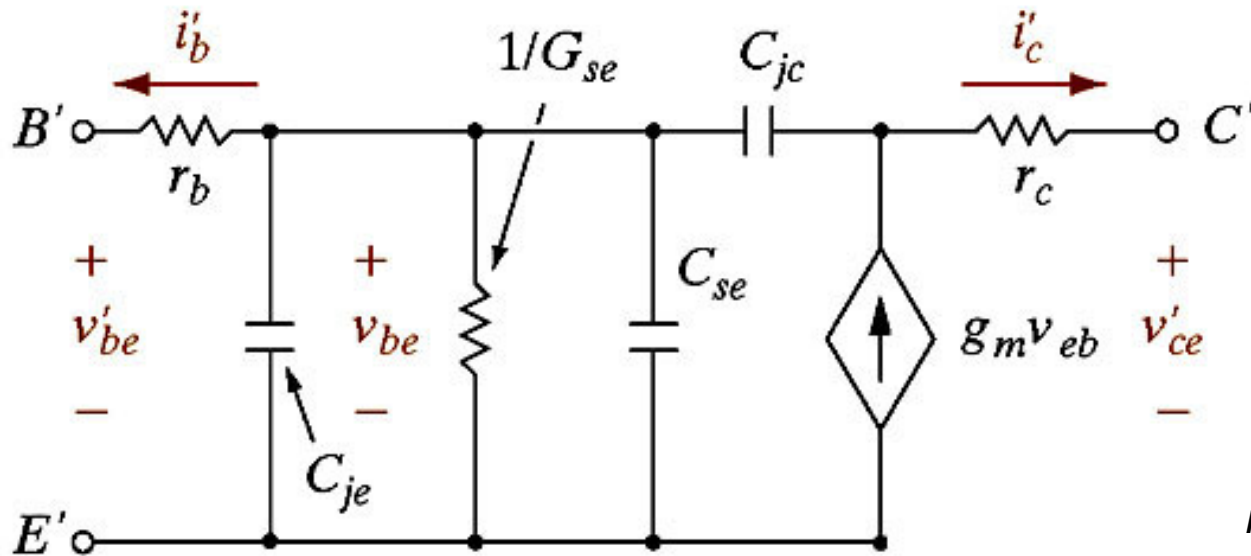
7.8 - Frequency Limits in BJT Amplification (Hybrid Pi), 7.7 – Advanced Stuff...

A low-noise Si bipolar transistor with $f_T = 8$ GHz. This device has 9 interdigitated emitter stripes, each 1 mm X 20 mm. (Photograph courtesy of Motorola.)



Worlds fastest transistor (2007)... is a BJT!





► Note: the model is only for normal forward active mode (amplification, not switching). There are other versions of this out there too...

► This is the Hybrid Pi model... can you tell me right now:

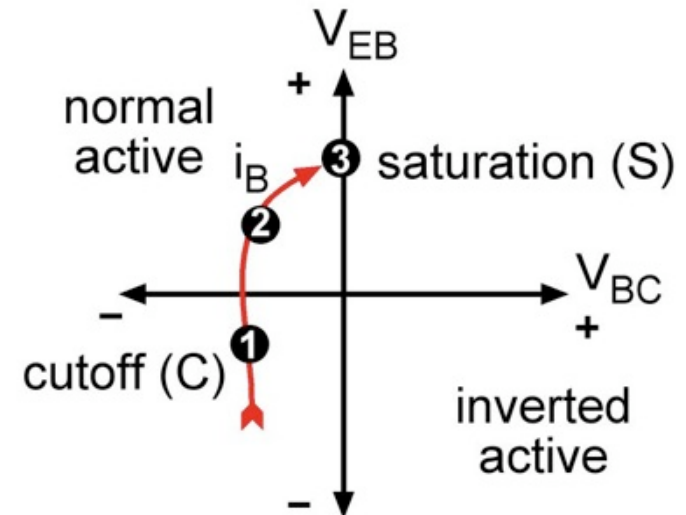
1) What single thing basically limits how fast you can drive any type of transistor?

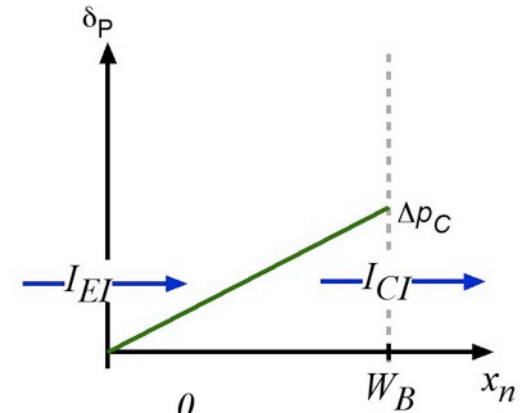
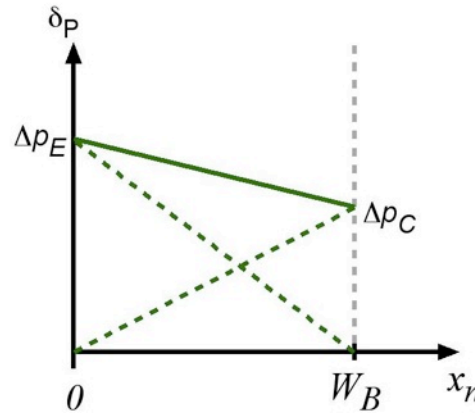
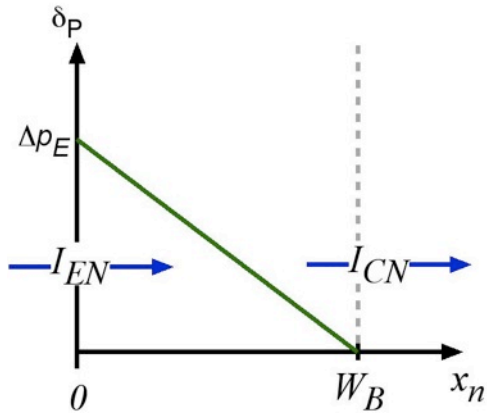
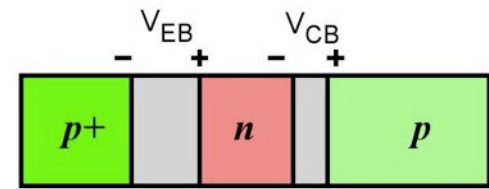
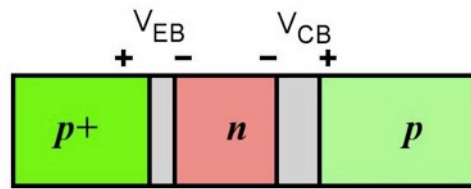
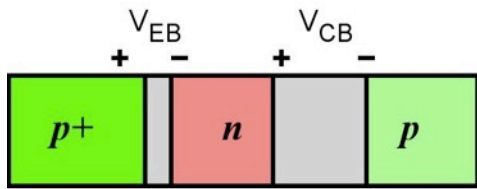
2) Tell me what each component does!

► For current source, is it different than the BJT in DC mode?

► What is g_m ? What units and what is it called and why?

► Why do we need both V_{be} and V_{ce} ?





▶ Lets look at one more approach to analyzing terminal currents: Charge Control Analysis... this approach is very useful for predicting BJT currents at high frequency

▶ Lets start where we started for deriving the Coupled Diode. Once again with subscript (N) refers to 'Normal Mode' and (I) to 'Inverted Mode'.

▶ Also, like before, we solve for (N) and (I) cases individually and then combine them to create the general case. Here we go again... but don't quit, I have a surprise for you!

Note... this is section 7.5.2 in the book (not section 7.8)

► Recall for the PN junction:

$$\tau_p = \frac{1}{\alpha_r(n_0 + p_0)}$$

$$L_p = \sqrt{D_p \tau_p}$$

$$D_p = \frac{kT}{q} \mu_p$$

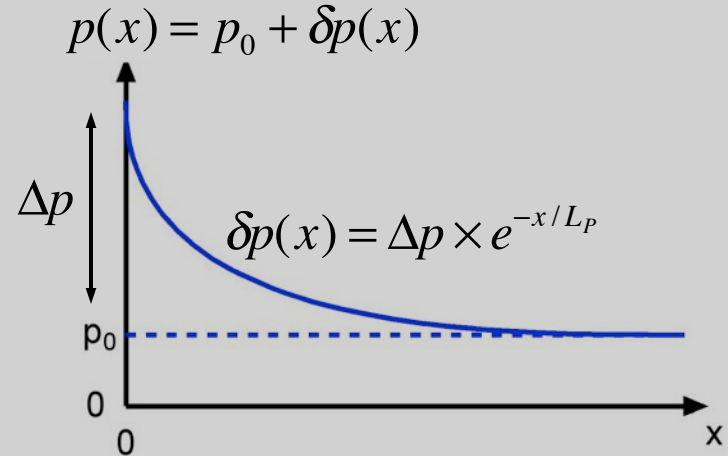
$$Q_p = q A \int_0^{\infty} \delta p(x_n) dx_n$$

$$= q A \Delta p_n \int_0^{\infty} e^{-x_n/L_p} dx_n$$

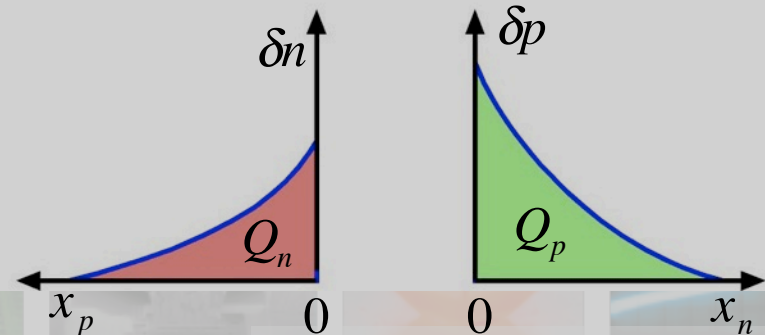
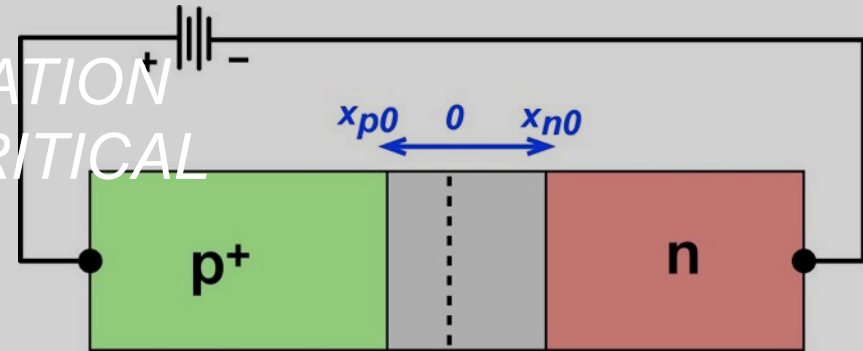
$$= q A \Delta p_n \left(0 - \frac{1}{1/-L_p} e^0 \right)$$

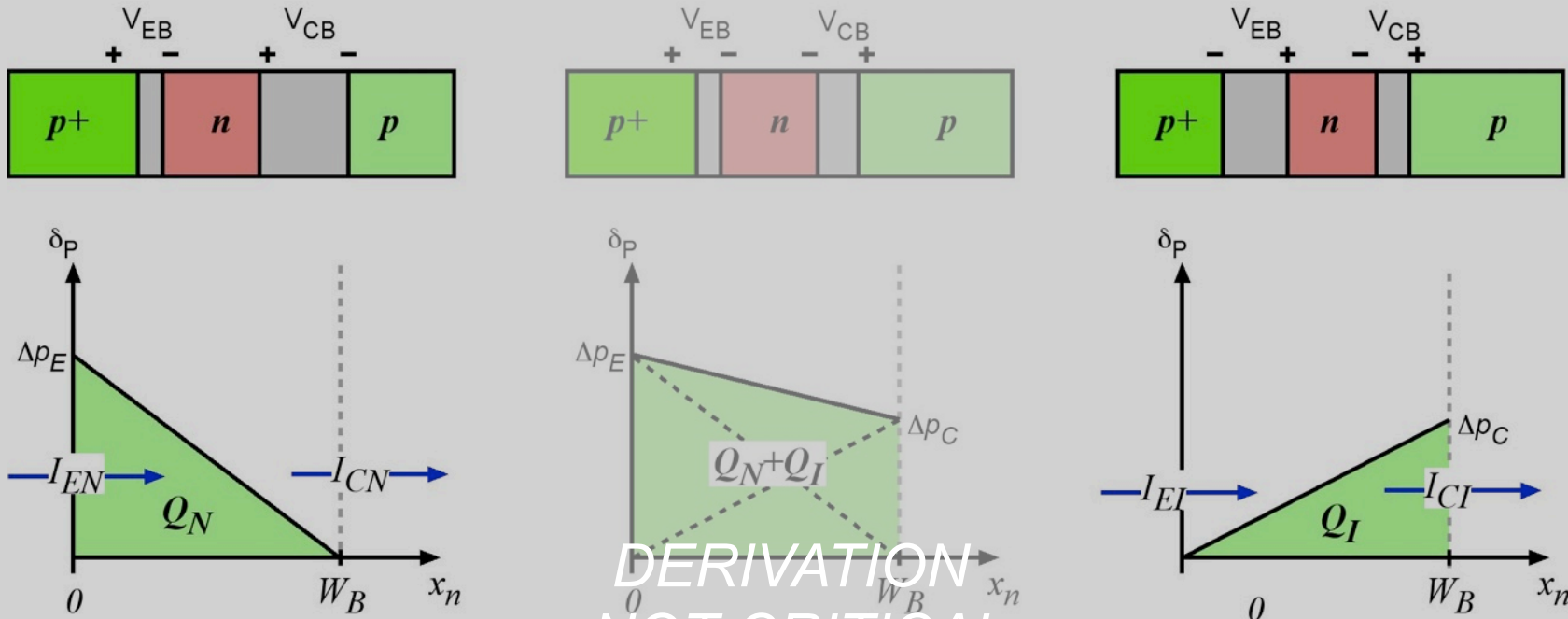
$$Q_p = q A \Delta p_n L_p$$

$$I_p(x_n = 0) = \frac{Q_p}{\tau_p}$$



DERIVATION NOT CRITICAL





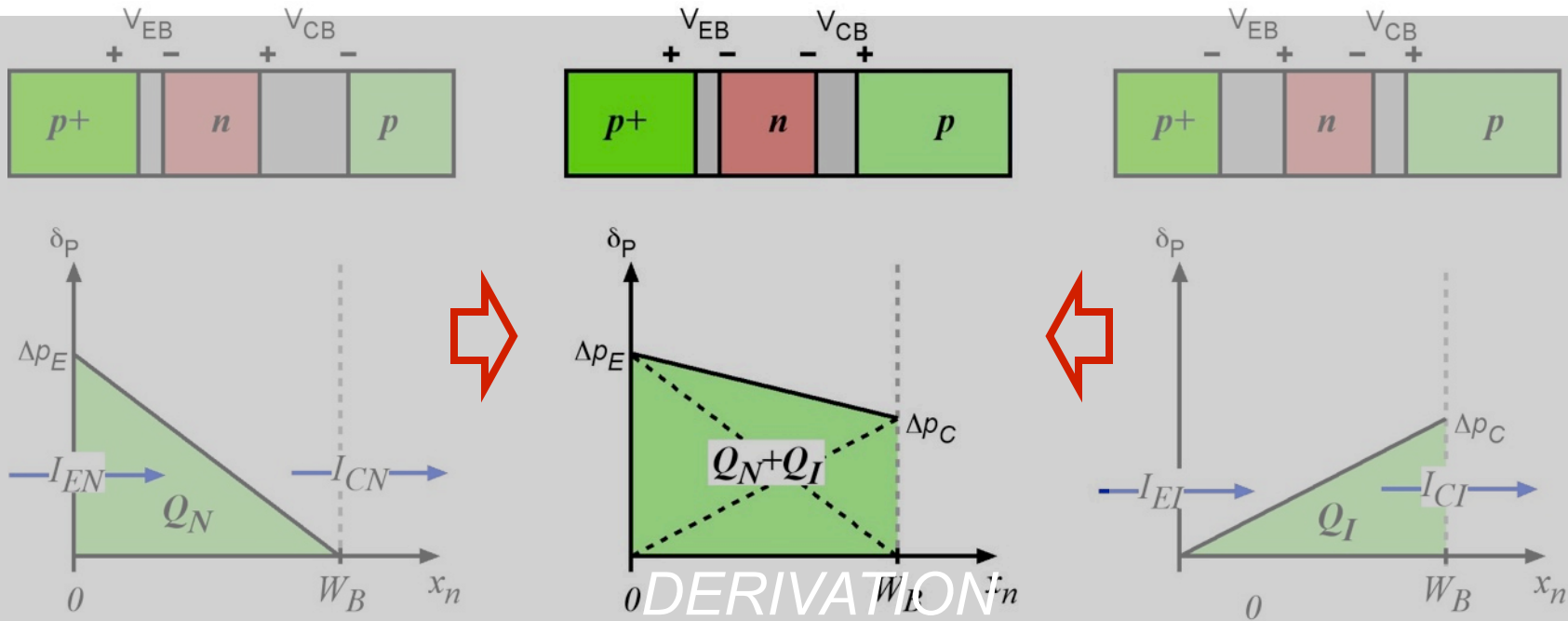
DERIVATION NOT CRITICAL

► Similar to that shown for the PN junction, the normal and inverted current components can be expressed in terms of the charge storage for normal (Q_N) and inverted (Q_I) cases (ignore center diagram above at first):

$$I_{EN} = \frac{Q_N}{\tau_{tN}} + \frac{Q_N}{\tau_{pN}} \quad , \quad I_{CN} = \frac{Q_N}{\tau_{tN}} \quad \quad I_{CI} = \frac{Q_I}{\tau_{tI}} + \frac{Q_I}{\tau_{pI}} \quad , \quad I_{EI} = \frac{Q_I}{\tau_{tI}}$$

τ_t transit time (or time required to collect all the charge)

τ_p recombination rate in the base (accounts for I_B !, look at eqs.. $I_C = I_E - I_B$)



DERIVATION NOT CRITICAL

► Now remember, we can add by superposition and include Normal and Inverted:

$$I_{CN} = \frac{Q_N}{\tau_{tN}} \quad , \quad I_{EN} = \frac{Q_N}{\tau_{tN}} + \frac{Q_N}{\tau_{pN}}$$

$$I_{EI} = \frac{Q_I}{\tau_{tI}} \quad , \quad I_{CI} = \frac{Q_I}{\tau_{tI}} + \frac{Q_I}{\tau_{pI}}$$



$$I_E = I_{EN} + I_{EI} = Q_N \left(\frac{1}{\tau_{tN}} + \frac{1}{\tau_{pN}} \right) - \frac{Q_I}{\tau_{tI}}$$

$$I_C = I_{CN} + I_{CI} = \frac{Q_N}{\tau_{tN}} - Q_I \left(\frac{1}{\tau_{tI}} + \frac{1}{\tau_{pI}} \right)$$



- ▶ The following relations can then be shown...

we will not derive, is like coupled diode with similar results! I_E , I_{ES} etc..

$$\alpha_N = \frac{\tau_{pN}}{\tau_{tN} + \tau_{pN}} \quad , \quad \alpha_I = \frac{\tau_{pI}}{\tau_{tI} + \tau_{pI}} \quad I_E = Q_N \left(\frac{1}{\tau_{tN}} + \frac{1}{\tau_{pN}} \right) - \frac{Q_I}{\tau_{tI}} \quad , \quad I_C = \frac{Q_N}{\tau_{tN}} - Q_I \left(\frac{1}{\tau_{tI}} + \frac{1}{\tau_{pI}} \right)$$

$$I_{ES} = q_N \left(\frac{1}{\tau_{tN}} + \frac{1}{\tau_{pN}} \right) \quad , \quad I_{CS} = q_I \left(\frac{1}{\tau_{tI}} + \frac{1}{\tau_{pI}} \right) \quad Q_N = q_N \frac{\Delta p_E}{p_n} \quad , \quad Q_I = q_I \frac{\Delta p_C}{p_n}$$

- ▶ The base current is obviously due to recombination, and amplification factor is simply recombination time divided by transit time (recall this analogy, how many carriers get through for each that recombine). For the normal mode these are then:

DERIVATION
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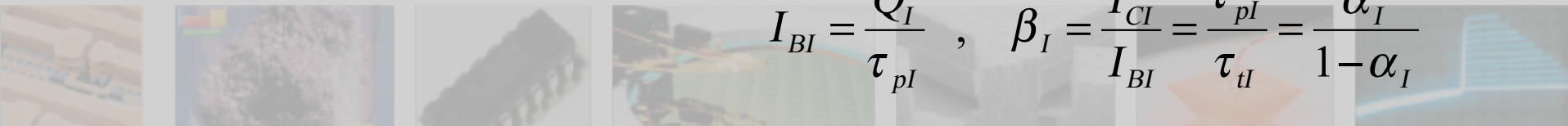
$$I_{CN} = \frac{Q_N}{\tau_{tN}} \quad \xrightarrow{\text{red arrow}}$$

$$\beta_N = \frac{I_{CN}}{I_{BN}} = \frac{\tau_{pN}}{\tau_{tN}} = \frac{\alpha_N}{1 - \alpha_N}$$

$$I_B = \frac{Q_N}{\tau_{pN}} \quad \xrightarrow{\text{red arrow}}$$

- ▶ And for inverted mode:

$$I_{BI} = \frac{Q_I}{\tau_{pI}} \quad , \quad \beta_I = \frac{I_{CI}}{I_{BI}} = \frac{\tau_{pI}}{\tau_{tI}} = \frac{\alpha_I}{1 - \alpha_I}$$



- Sum the results (superposition, once again) to get the total base current:

$$I_B = \frac{Q_N}{\tau_{pN}} \quad I_{BI} = \frac{Q_I}{\tau_{pI}} \quad \rightarrow \quad I_B = I_{BN} + I_{BI} = \frac{Q_N}{\tau_{pN}} + \frac{Q_I}{\tau_{pI}}$$

- To summarize, we can express all three components in steady state as:

$$I_B = \frac{Q_N}{\tau_{pN}} + \frac{Q_I}{\tau_{pI}}$$

$$I_E = Q_N \left(\frac{1}{\tau_{tN}} + \frac{1}{\tau_{pN}} \right) - \frac{Q_I}{\tau_{tI}}$$

$$I_C = \frac{Q_N}{\tau_{tN}} - Q_I \left(\frac{1}{\tau_{tI}} + \frac{1}{\tau_{pI}} \right)$$

Another way to express currents!

- Lastly, to include time dependence we need to take into consideration current component that is induced after we rapidly switch the transistor and charge storage

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must be changed... lower case = AC

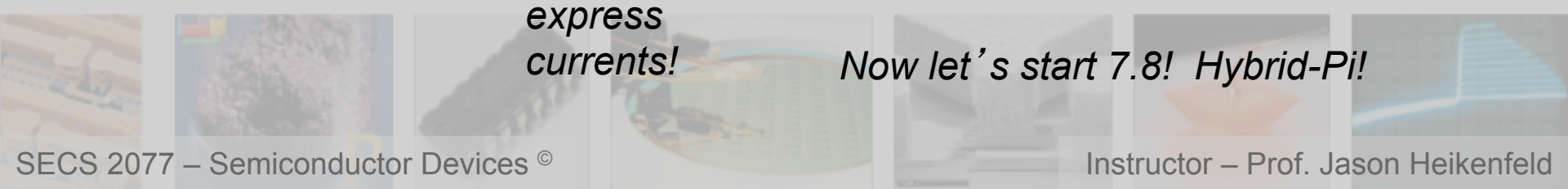
$$i_B = I_B + \frac{dQ_N}{dt} + \frac{dQ_I}{dt}$$

$$i_E = I_E + \frac{dQ_N}{dt}$$

$$i_C = I_C - \frac{dQ_I}{dt}$$

why i_E only Q_N and i_C only Q_I ? Charge storage only for forward bias junction!

Now let's start 7.8! Hybrid-Pi!



► In lect. 7-4 we showed that:

$$I_B \approx \frac{Q_p}{\tau_p} \quad Q_p = \frac{1}{2} qA\Delta p_E W_b$$

$$I_B \approx \frac{qAW_b\Delta p_E}{2\tau_p}$$

► If we add a small AC signal v_{eb} on top of our DC signal V_{EB} ICBST:

$$\Delta p_E \approx p_n e^{qV_{EB}/kT}$$

$$\Delta p_E(t) \cong \Delta p_E \left(1 + \frac{qv_{eb}}{kT} \right)$$

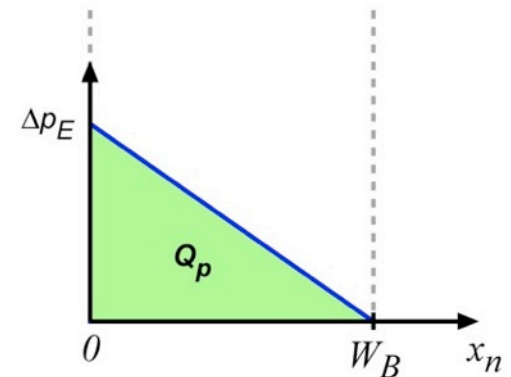
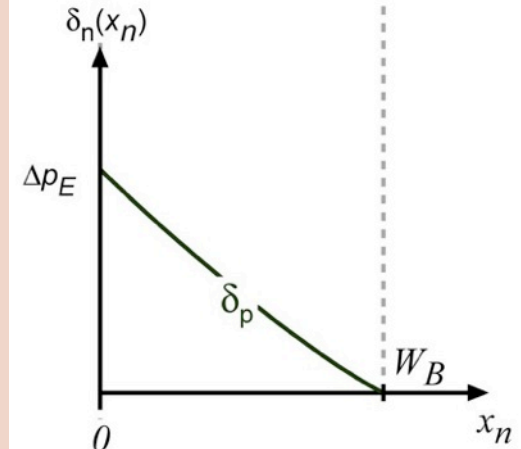
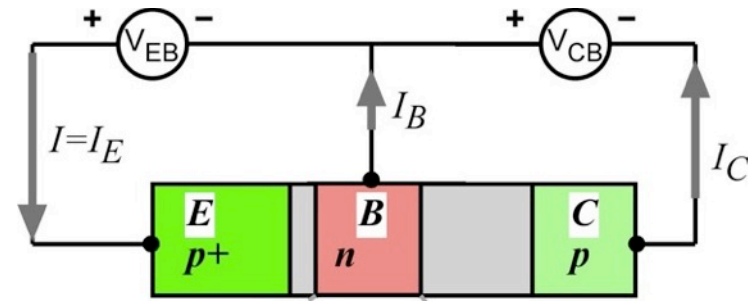
$$Q_p = \frac{1}{2} qA\Delta p_E(t)W_b$$

Assumes locally linear response...

So... again, what is transconductance?

Notice that the effect of V_{EB} increases as the DC portion of I_B increases (is proportional)...

...so our our small signal transconductance is also proportional to I_B .



continue on next slide..

$$Q_N(t) = \frac{1}{2} q A \Delta p_E(t) = \frac{1}{2} q A \Delta p_E \left(1 + \frac{q v_{eb}}{kT} \right)$$

Remember: $I_B \approx \frac{Q_p}{\tau_p}$ $Q_p \approx I_B \tau_p$

Change terminology for the pnp BJT in normal forward mode ($Q_p=Q_N$), and rework...

$$Q_N(t) = I_B \tau_p \left(1 + \frac{q v_{eb}}{kT} \right)$$

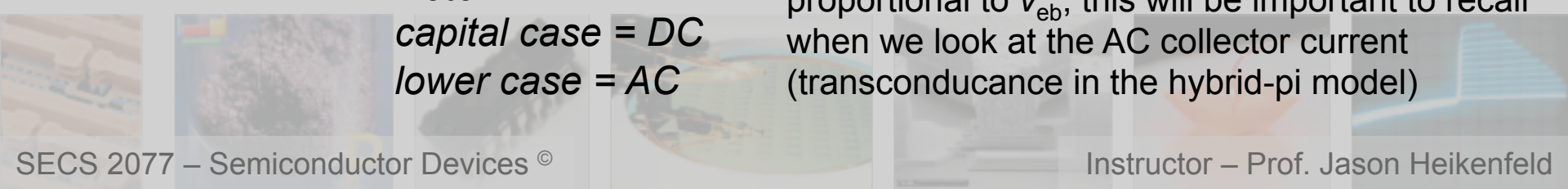
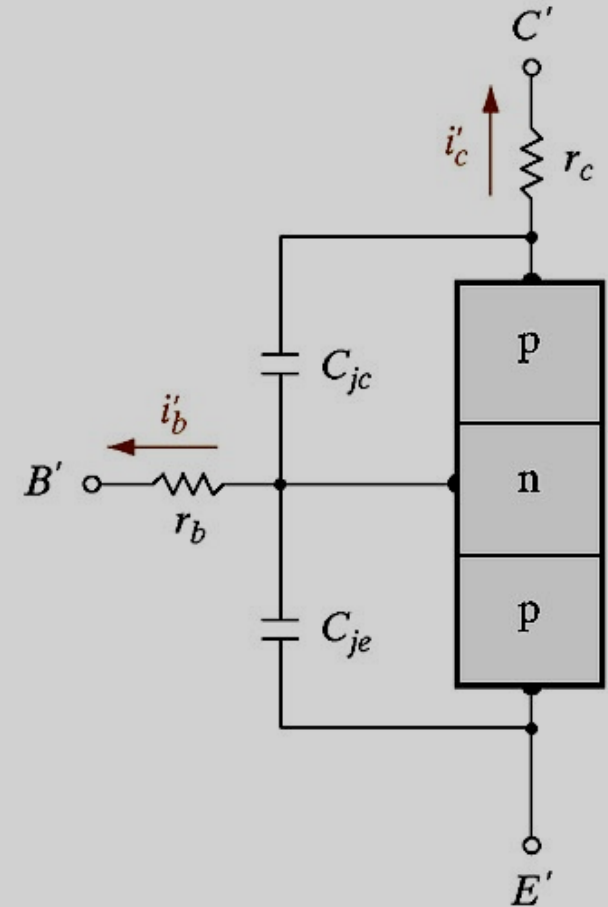
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We can therefore obtain i_b as DC + AC components...

$$i_b(t) = \frac{Q_N(t)}{\tau_p} + \frac{dQ_N(t)}{dt}$$

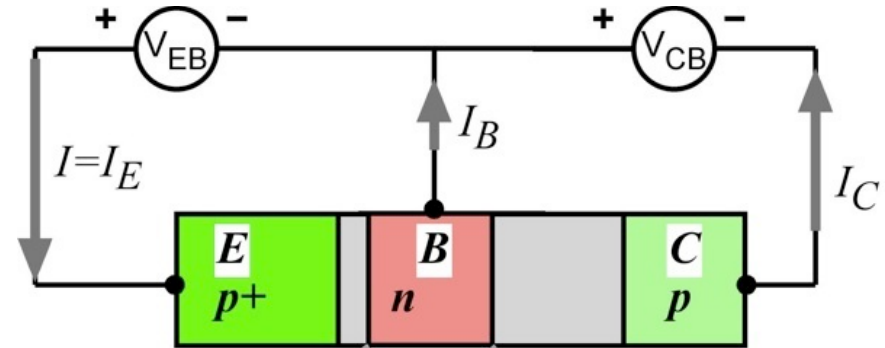
Note:
capital case = DC
lower case = AC

Also take note, holes into base only linearly proportional to v_{eb} , this will be important to recall when we look at the AC collector current (transconductance in the hybrid-pi model)



$$C = \frac{Q}{V} = \left| \frac{dQ}{dV} \right| = \frac{\epsilon_0 \epsilon_r A}{d}$$

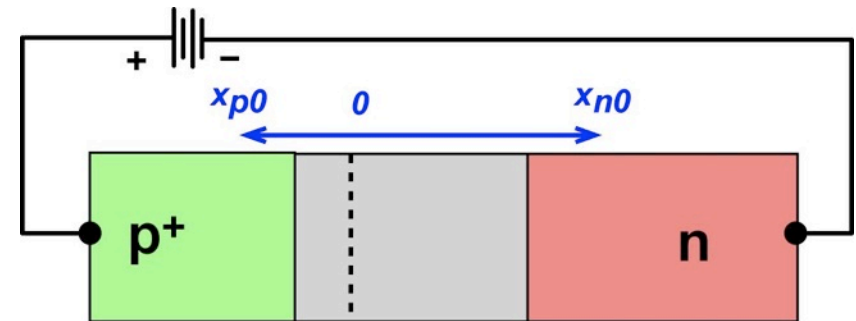
Which junctions do we care about for capacitance when modulating the BJT in high frequency AC mode? Also, what 2 types of capacitance?



► Capacitance #1:

- depletion or junction capacitance (C_j)
- where is the 'dielectric'
- how change w/ V ?

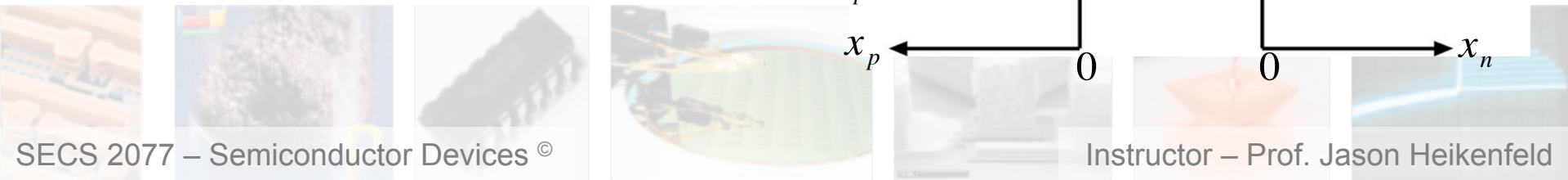
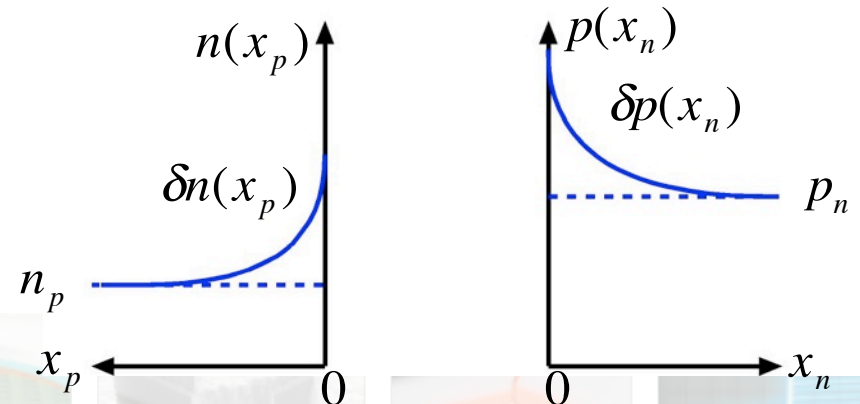
$$C_j = \frac{\epsilon_0 \epsilon_{Si} A}{W}$$



► Capacitance #2:

- storage capacitance (C_s)
- minority carriers
- see how changes with V ...
- so how will it change with I_B ?

$$C_s = \frac{dQ}{dV} \propto e^{qV/kT}$$



- ▶ Using what was shown in section 5.5.4 (‘short diode’) the ICBST:

$$\rightarrow i_b(t) = \frac{Q_N(t)}{\tau_p} + \frac{dQ_N(t)}{dt}$$

$$\rightarrow i_b(t) = I_B + \frac{q}{kT} I_B v_{eb} + \frac{2}{3} \frac{q}{kT} I_B \tau_p \frac{dv_{eb}}{dt}$$

- ▶ We can re-arrange terms and write the a-c component of $i_b(t)$ to be:

DERIVATION
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$$i_b = G_{se} v_{eb} + C_{se} \frac{dv_{eb}(t)}{dt}$$

where

$$G_{se} \equiv \frac{q}{kT} I_B \quad \text{and} \quad C_{se} \equiv \frac{2}{3} \frac{q}{kT} I_B \tau_p = \frac{2}{3} G_{se} \tau_p$$

thus an a-c conductance (G_{se}) and capacitance are associated with the B-E junction due to charge storage (C_{se}) effects



► Further using charge control analysis developed in 7-5, we can similarly derive the AC component of the collector current:

$$I_{CN} = \frac{Q_N}{\tau_{tN}}, \quad I_{EN} = \frac{Q_N}{\tau_{tN}} + \frac{Q_N}{\tau_{pN}} \quad Q_N(t) = I_B \tau_p \left(1 + \frac{qV_{eb}}{kT} \right)$$

τ_t transit time (or time required to collect all the charge)

τ_p recombination rate in the base

➔ $i_c(t) = \frac{Q_N(t)}{\tau_t} = \beta I_B + \frac{q}{kT} \beta I_B V_{eb}$ *DERIVATION NOT CRITICAL or in more convenient form:*

➔ $i_c = g_m V_{eb}$

where

➔ $g_m \equiv \frac{q}{kT} \beta I_B = \frac{3}{2} \frac{C_{se}}{\tau_t}$

► The quantity g_m is the a-c transconductance... lets combine these to form a simple circuit model (the famous hybrid-pi model)...



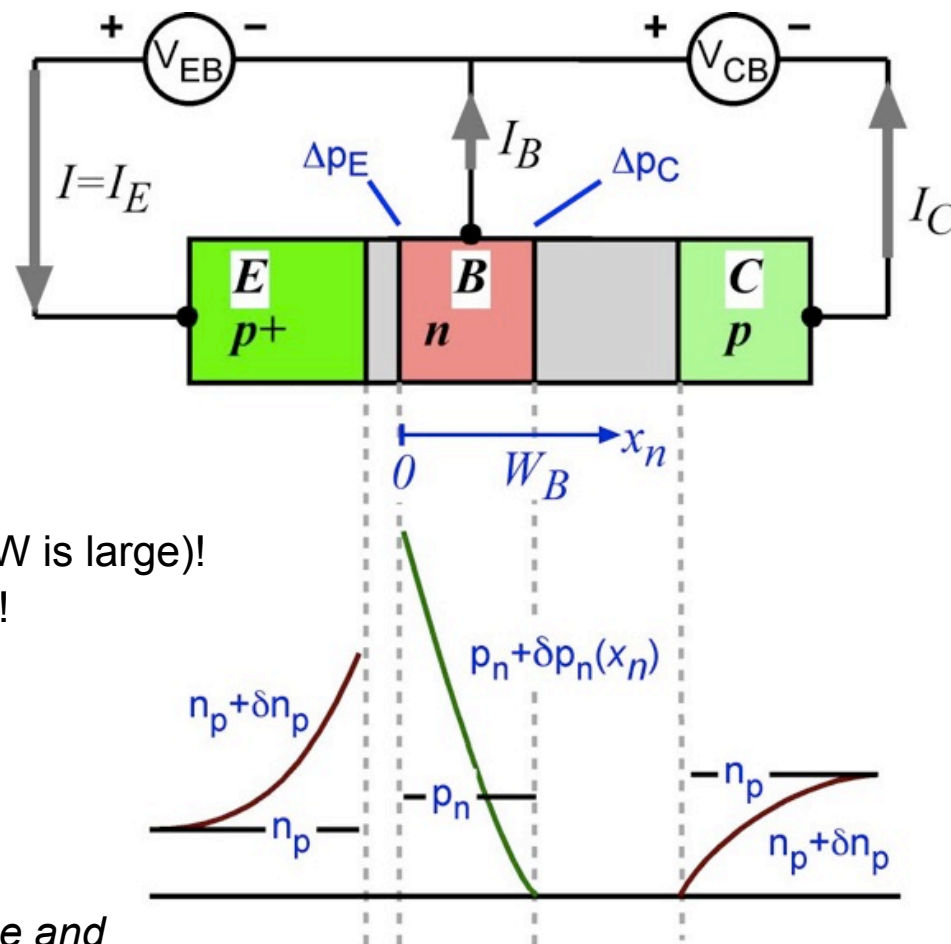
▶ Okay, lets review the capacitances we see one more time... Then we are ready!

For each terminal of our hybrid Pi model we should see some capacitance, right?

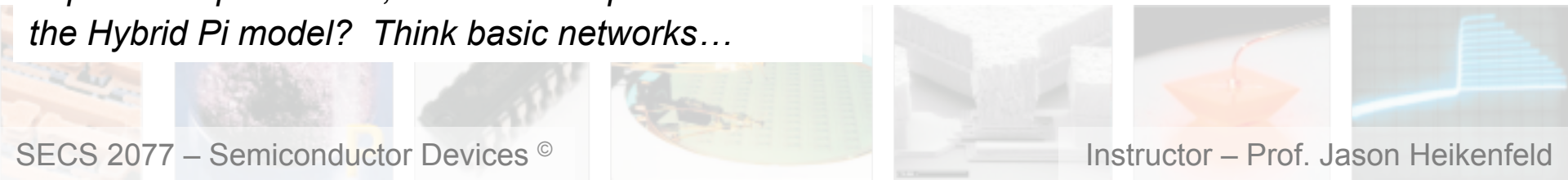
- ▶ Looking in from the emitter:
 - we have large EB depletion capacitance (W is small)!
 - we have large storage capacitance since is in forward bias...

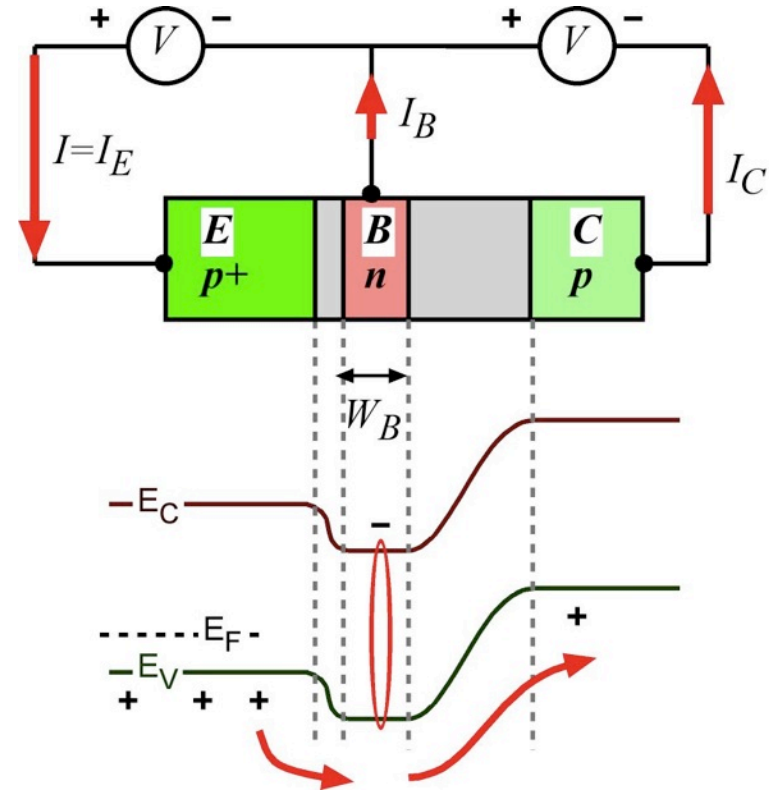
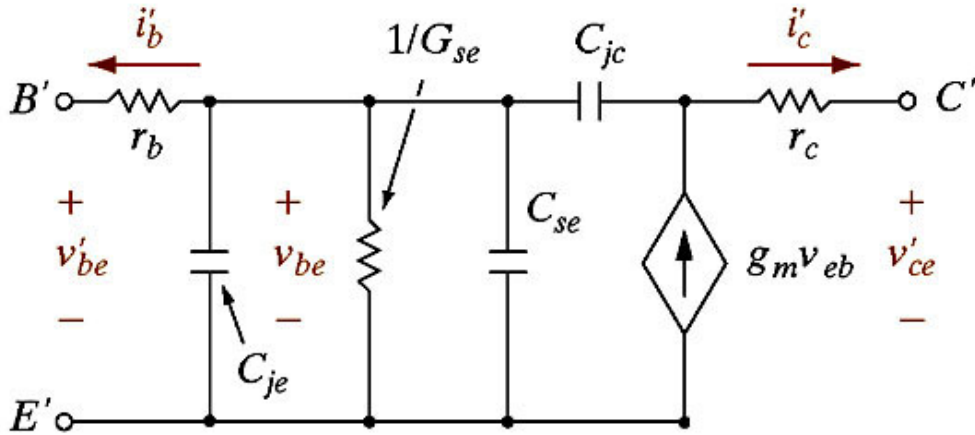
- ▶ Looking in from the collector:
 - we have small BC depletion capacitance (W is large)!
 - no storage capacitance... reverse biased!

- ▶ Looking in from the base:
 - see both EB and BC depletion caps
 - *and* large storage EB capacitance!



If both the base and emitter see both EB storage and depletion capacitances, how should I place them in the Hybrid Pi model? Think basic networks...

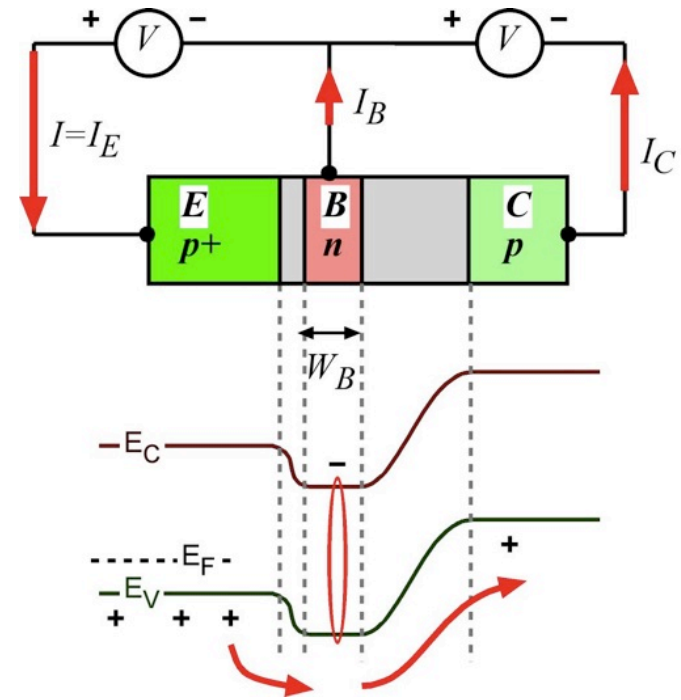
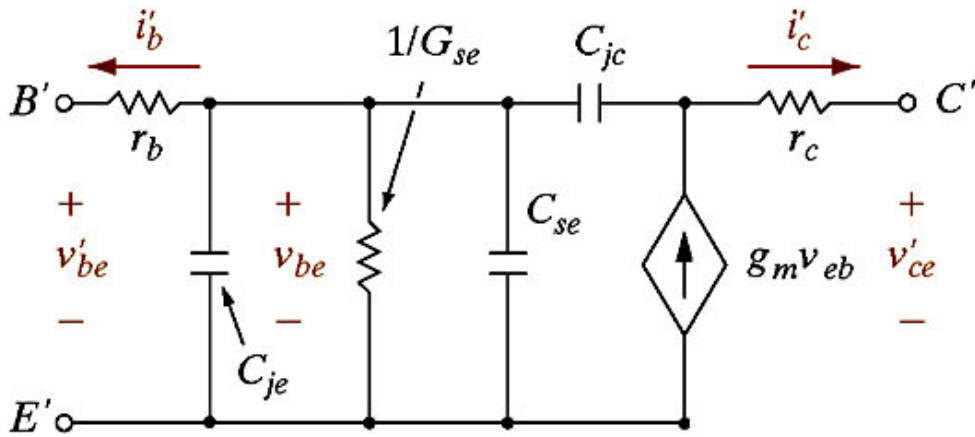




- ▶ We put the resistors in place...
- ▶ We put the base recomb. in place ($1/G_{SE}$)
- ▶ We put the capacitors in place...
- ▶ We put the small signal collector current in place...
-remember, we showed was proportional to g_m

$$i_c = g_m v_{eb} \quad i_b = G_{se} v_{eb} + C_{se} \frac{dv_{eb}(t)}{dt}$$

$$g_m = \frac{3 C_{se}}{2 \tau_t} \quad G_{se} \equiv \frac{q}{kT} I_B$$



▶ Look at terminal resistances:

- ★ -there is an r_b ... why? *think geometry*
 - there is an r_c ... why?
 - there is no r_e ... why? *doping and diode*
- all are easy to calculate ($J = q \mu p_o E$)*

▶ Next find EB, BC depletion capacitance

★ $C_j = \frac{\epsilon A}{W}$

▶ What is this $1/G_{se}$ term? ★

- what is unit for q/kT (think of units for G)
- between BE but not BC? $G_{se} \equiv \frac{q}{kT} I_B$
- why proportional to I_B ?

▶ Where is our storage capacitance?

- why between BE but not BC?
- effect of T, I_B, τ_p ?

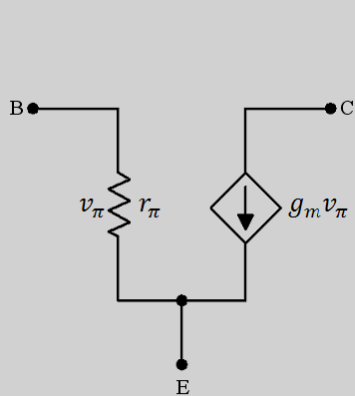
★ $C_{se} \equiv \frac{2}{3} \frac{q}{kT} I_B \tau_p$

▶ Lastely $g_m v_{eb}$? ★

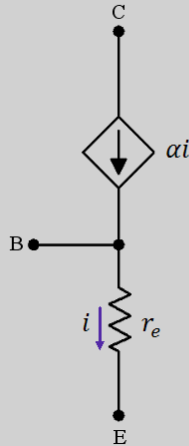
- **transconductance!** $g_m \equiv \frac{q}{kT} \beta I_B = \frac{3}{2} \frac{C_{se}}{\tau_t} \quad \frac{1}{R} = \frac{I}{V}$

EB diode, more forward bias, higher up on $e^{qV/kt}$, therefore larger change in i_c to v_{eb}

The Hybrid-Pi Model



The T Model



Great find. Okay here we go:

I can see on the diagram that they are working with an npn (not pnp).

So the current should be in the opposite direction (electrons flowing from left to right, is current direction in the other direction).

Now, the voltage gain shows a 180 degree phase shift.

If npn I am feeding holes into the base (positive current into the base). That makes v(pi) positive too. Therefore the current source should be negative (current direction for the collector is into the BJT collector). That gives a negative voltage drop across RL if I reference everything to ground.

Make sense?

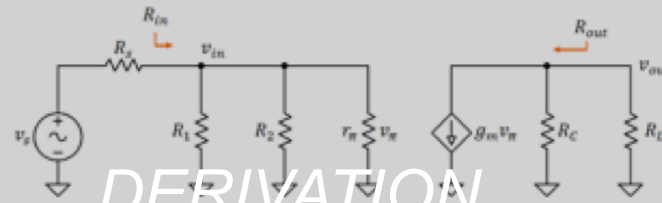
Stop by if need be. I am not certain of my answer (just did this for the 1st time). Bring your circuits in question and we can look at them together...

-JCH

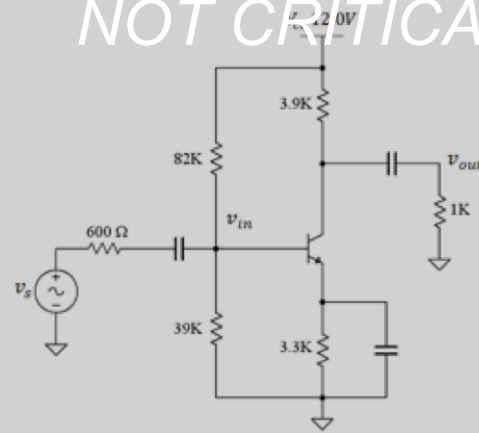
Jason Heikenfeld, CEAS '98
 Assoc. Professor & Director, Novel Devices Laboratory
 School of Electronics and Computing Systems, University of Cincinnati
 www.ece.uc.edu/devices / 513-556-4763

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$$A_v = \frac{v_{out}}{v_{in}} = -g_m(R_C || R_L)$$



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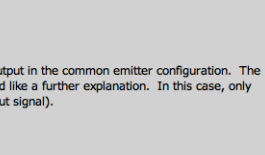
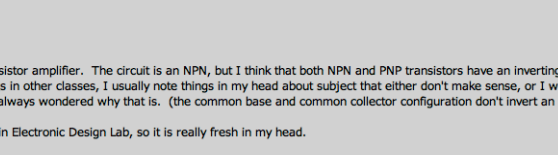
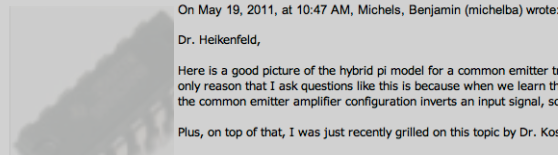
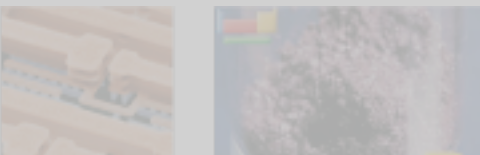
On May 19, 2011, at 10:47 AM, Michels, Benjamin (michelba) wrote:

Dr. Heikenfeld,

Here is a good picture of the hybrid pi model for a common emitter transistor amplifier. The circuit is an NPN, but I think that both NPN and PNP transistors have an inverting output in the common emitter configuration. The only reason that I ask questions like this is because when we learn things in other classes, I usually note things in my head about subject that either don't make sense, or I would like a further explanation. In this case, only the common emitter amplifier configuration inverts an input signal, so I always wondered why that is. (the common base and common collector configuration don't invert an input signal).

Plus, on top of that, I was just recently grilled on this topic by Dr. Kosel in Electronic Design Lab, so it is really fresh in my head.

<http://circuitspot.com/?p=529>



▶ ICBST that combining effects of C_j and C_s the cutoff frequency for unity gain ($\beta=1$) of the BJT is related to a single delay time (τ_d):

$$f_T = \frac{1}{2\pi\tau_d}$$

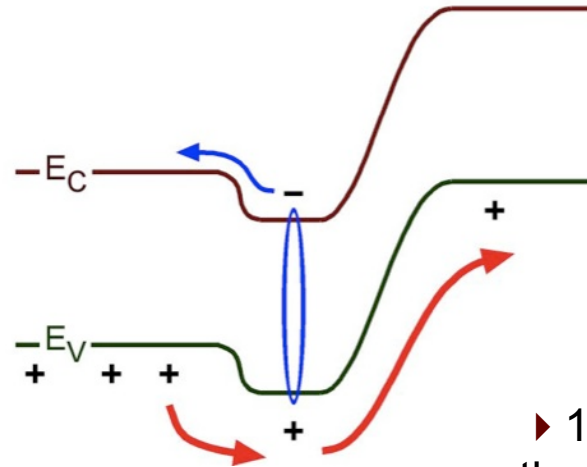
▶ BJTs can be designed such that storage and junction capacitance are not the limiting factor for the switching speed...

▶ Ultimate fundamental limit is that of the base transit time (τ_t)...

$$\rightarrow I_{Ep} \approx qA \frac{D_p}{L_p} \Delta p_E \operatorname{ctnh} \frac{W_b}{L_p}$$

$$\rightarrow I_C \approx qA \frac{D_p}{L_p} \Delta p_E \operatorname{csch} \frac{W_b}{L_p}$$

$$\rightarrow I_B \approx qA \frac{D_p}{L_p} \Delta p_E \operatorname{tanh} \frac{W_b}{2L_p}$$



▶ Why D_p on bottom?
Why W_b^2 on top? ☆

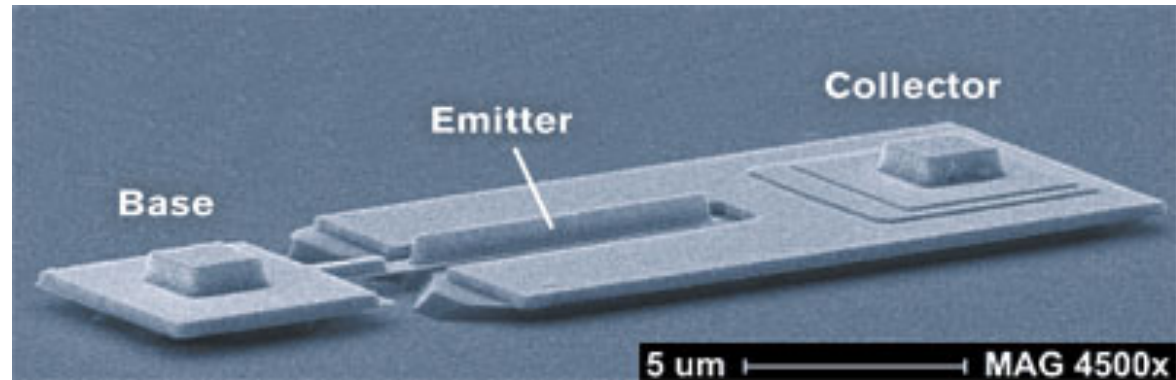
▶ 1st W_b is for 'speed' (C/s), the 2nd for 'distance'!

$$\rightarrow \beta = \frac{I_C}{I_B} \cong \frac{\operatorname{csch} W_b/L_p}{\operatorname{tanh} W_b/2L_p} = \frac{2L_p^2}{W_b^2} = \frac{2D_p\tau_p}{W_b^2} = \frac{\tau_p}{\tau_t}$$

$$\therefore \tau_t = \frac{W_b^2}{2D_p}$$



Clocking in at 845 GHz, the transistor is fabricated with InP and GaAs, and employs pseudomorphic grading of the base and collector regions. (Source: University of Illinois)



Dec. 2006 - Scientists at the University of Illinois at Urbana-Champaign have again broken their own speed record for the **world's fastest transistor**. With a frequency of 845 GHz, their latest device is ~300 GHz faster than transistors built by other research groups, and approaches the goal of a **terahertz device**.

Made from indium phosphide and indium gallium arsenide, “The new transistor utilizes a pseudomorphic grading of the base and collector regions,” said Milton Feng, Holonyak Chair Professor of electrical and computer engineering at U of I. “The compositional grading of these components enhances the electron velocity, hence, reduces both current density and charging time.”

With this latest device, Feng and his research group have taken the transistor to a new range of high-speed operation, finally bringing the “Holy Grail” of a terahertz transistor within reach. In addition to using pseudomorphic material construction, the researchers also refined their fabrication process to produce tinier transistor components. For example, the transistor's base is only 12.5 nm.

Clocking in at 845 GHz, the transistor is fabricated with InP and GaAs, and employs pseudomorphic grading of the base and collector regions. (Source: University of Illinois)

“By scaling the device vertically, we have reduced the distance electrons have to travel, resulting in an increase in transistor speed,” said graduate student William Snodgrass, who described the new device at the International Electronics Device Meeting (IEDM), held in San Francisco Dec. 11-13. “Because the size of the collector has also been reduced laterally, the transistor can charge and discharge faster.”



▶ Why do we need the hybrid Pi model?
Don't need it, for DC bias, or for understanding the AC frequency limit.

▶ Why do we need both V'_{be} and V_{be} ?
Hint, you apply a voltage to the BJT, but that does not mean the emitter/base charges up instantly to that applied voltage...

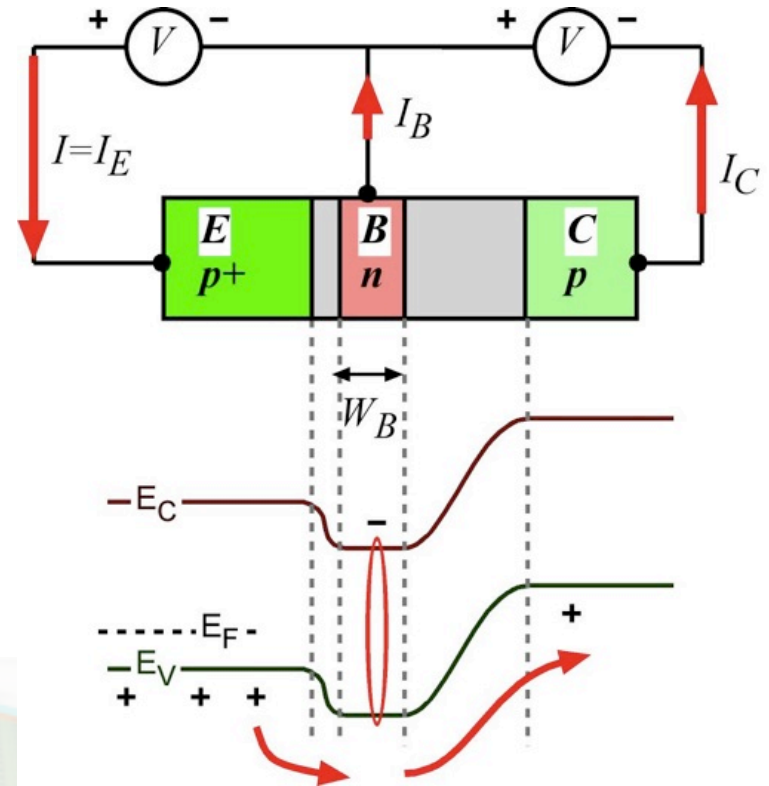
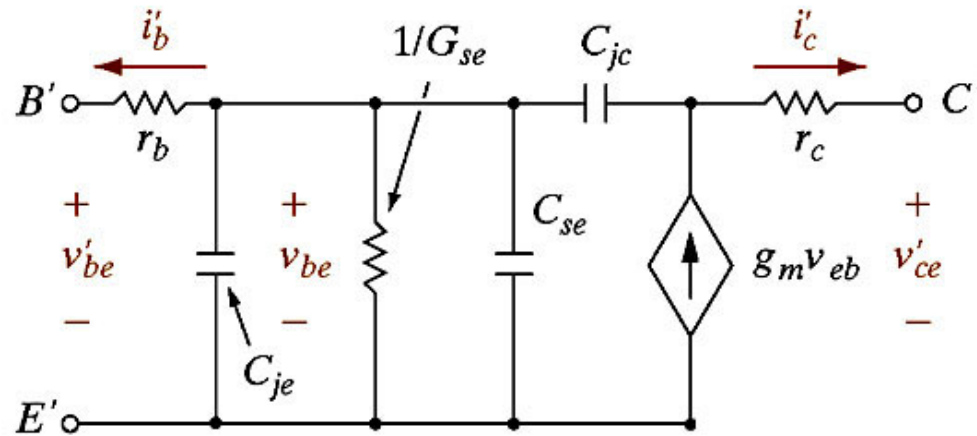
▶ Why r_b ? Hint, thin doping & geometry.

▶ Why $1/G_{SE}$? Hint, this accounts for why we need base current...

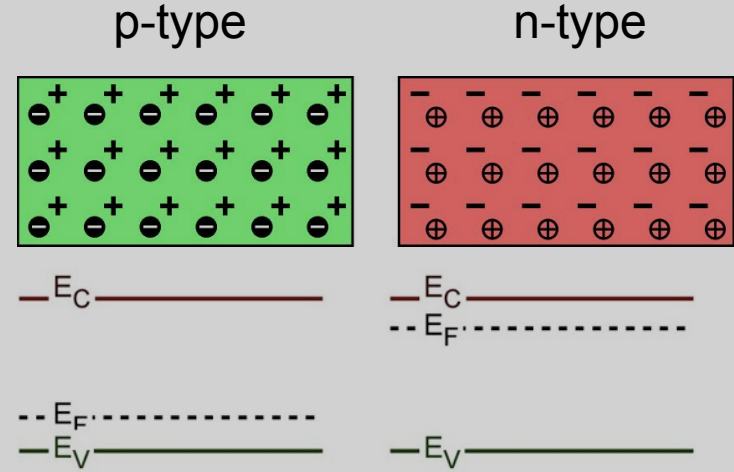
▶ What are the capacitances and how do they change with voltage? Hint, one is for reverse bias and two are for forward bias...

▶ Why does g_m increase with I_B ? Hint, think of where increased I_B puts you on the diode exponential and the local slope...

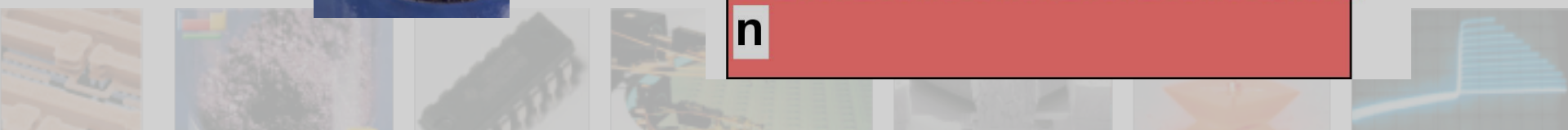
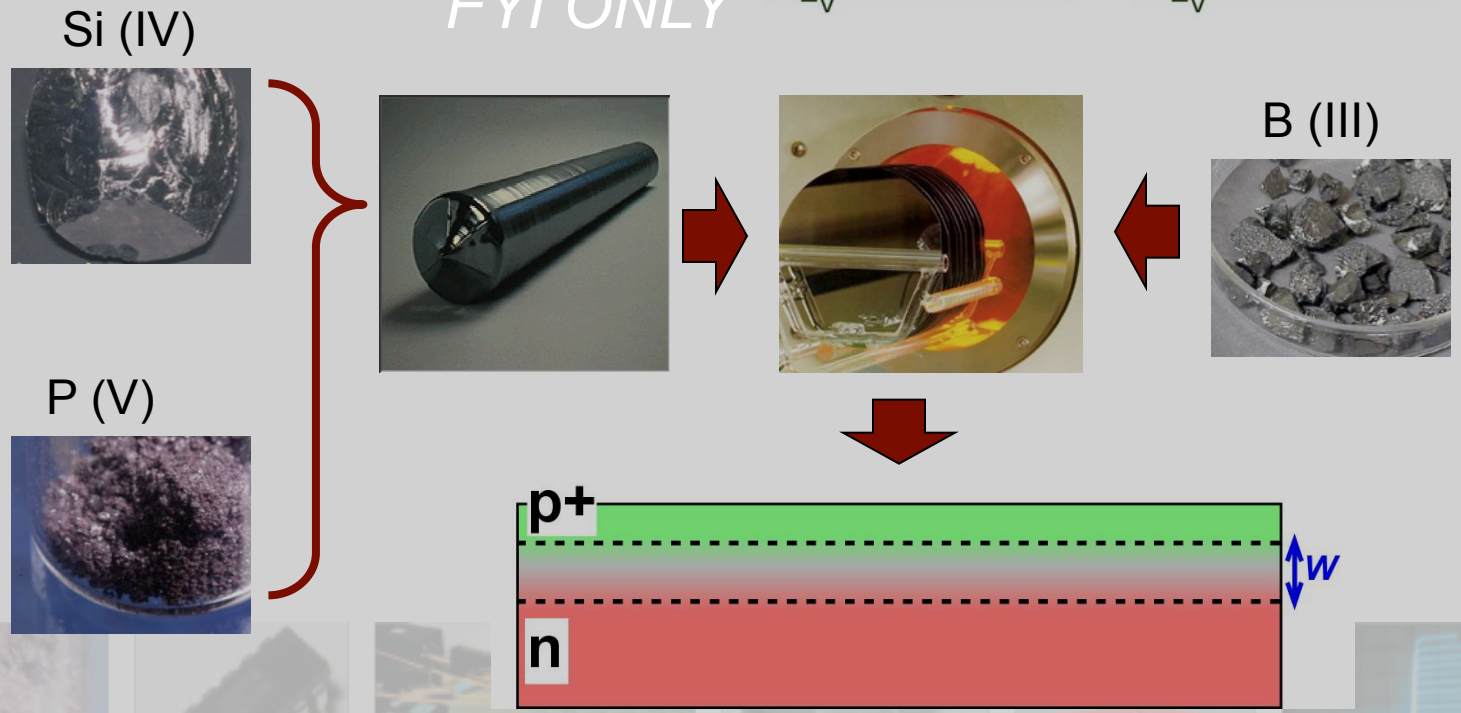
▶ What is the frequency limit for a BJT determined by, at the absolute limit, and what parameters control that?



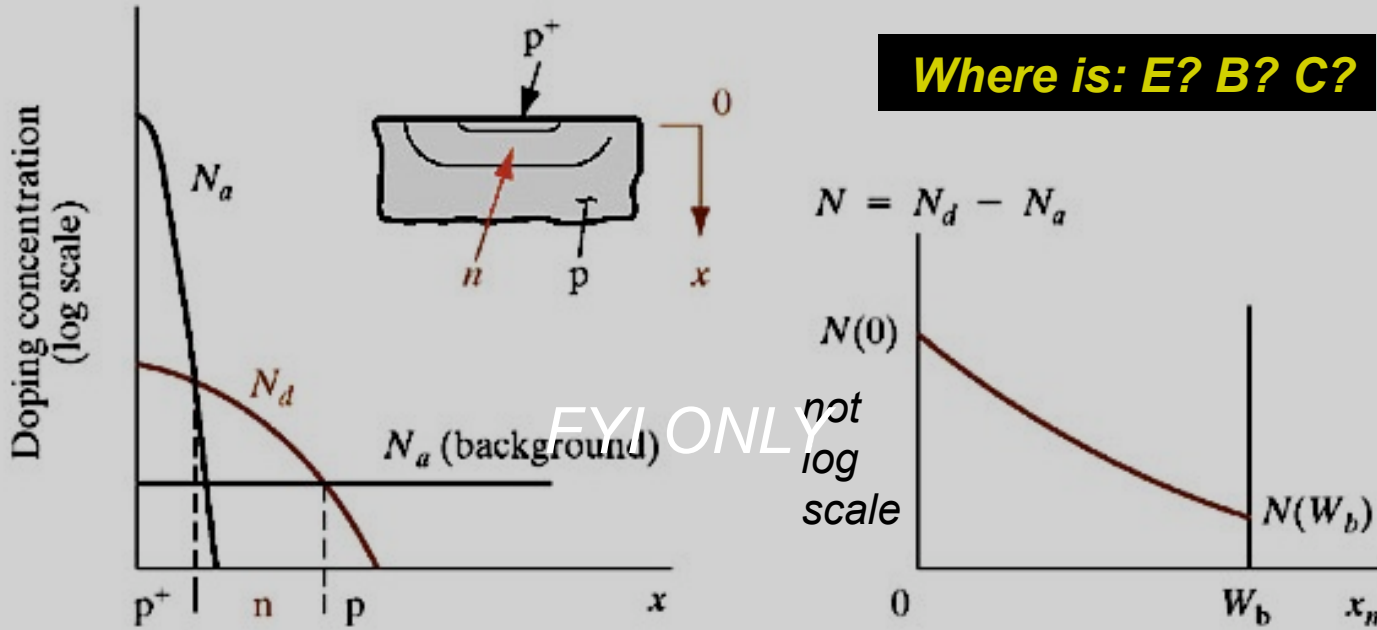
- ▶ Lets move onto some advanced topics for BJTs in general...
- ▶ So far we have assumed our BJTs are formed like this:
- ▶ It is simpler to make an n-type (or p-type) Si wafer and diffuse in dopants



FYI ONLY



- ▶ However, dopant diffusion gives use doping profiles:

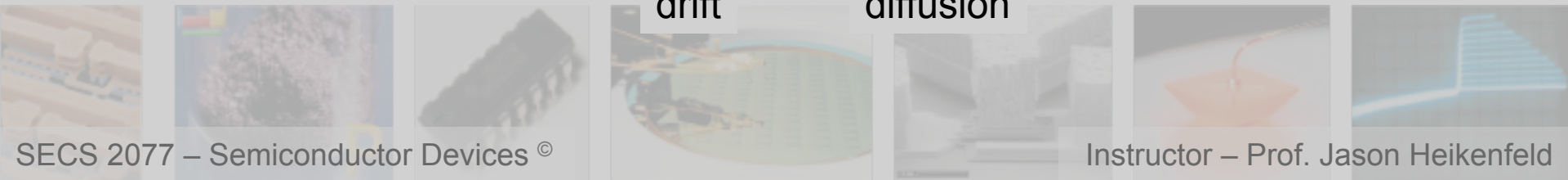


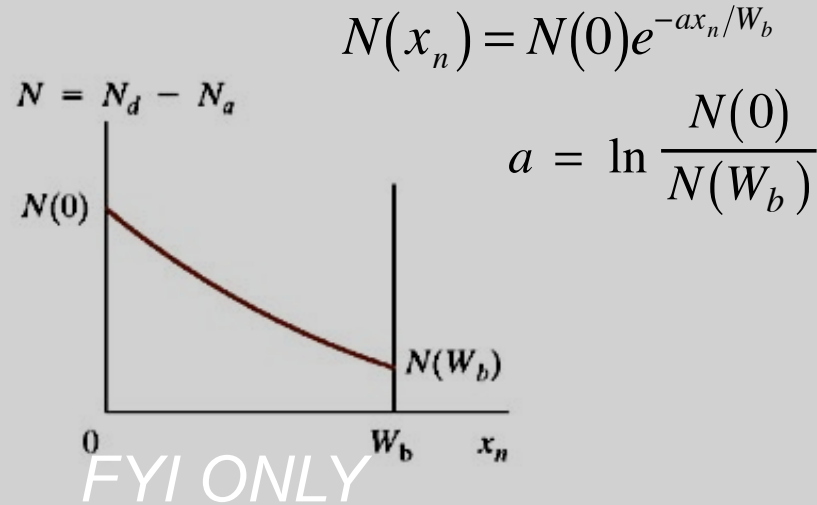
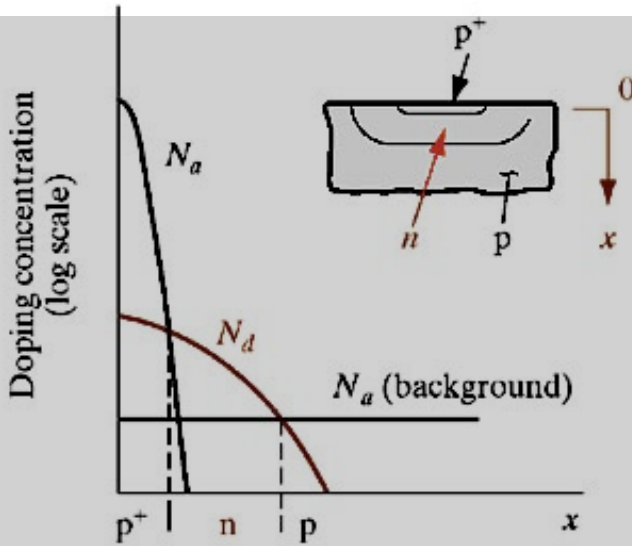
- ▶ This will effect our BJT performance... (in a good way!) Any guesses?
- ▶ First, go back to general equation for current density in **uniformly doped** n-type S/C:

$$J_n(x) = q\mu_n n(x)E(x) + qD_n \frac{dn(x)}{dx}$$

drift

diffusion





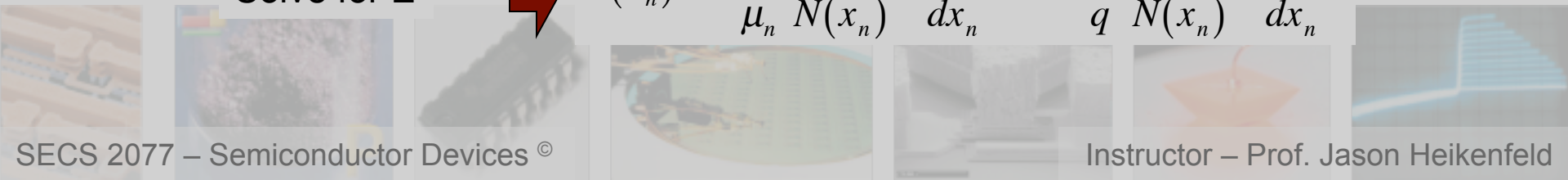
➔
$$J_n(x) = q\mu_n n(x)E(x) + qD_n \frac{dn(x)}{dx}$$

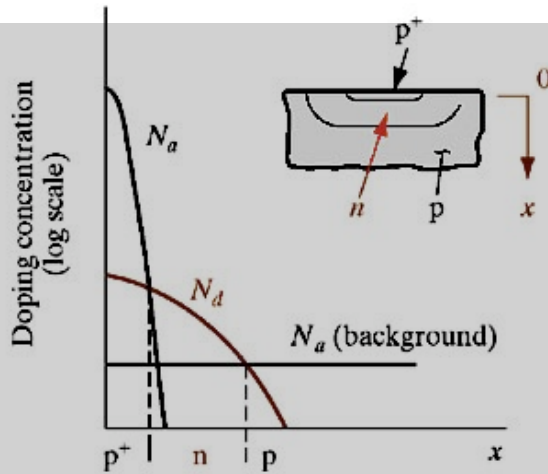
▶ For the BJT above we can assume $n(x_n) = N_D(x_n)$ at 300K and that $I=0$ at therm. equil.

➔
$$I_n(x_n) = qA\mu_n N(x_n)E(x_n) + qD_n \frac{dn(x_n)}{dx} = 0$$

Solve for E

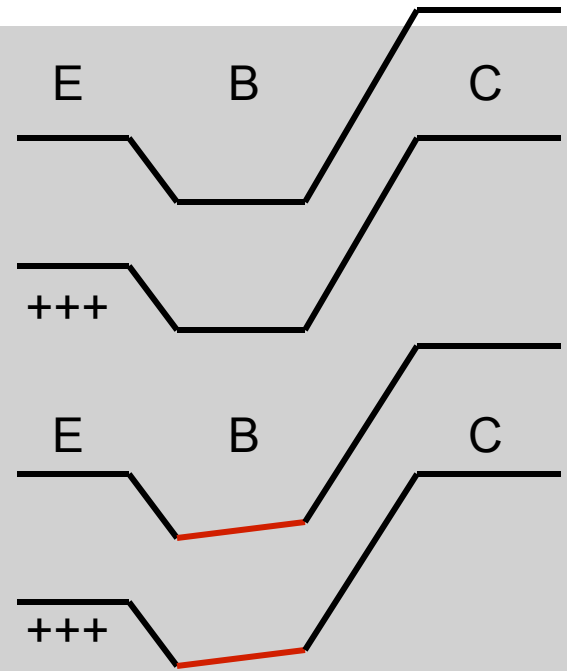
➔
$$E(x_n) = -\frac{D_n}{\mu_n} \frac{1}{N(x_n)} \frac{dN(x_n)}{dx_n} = -\frac{kT}{q} \frac{1}{N(x_n)} \frac{dN(x_n)}{dx_n}$$





$$E(x_n) = -\frac{kT}{q} \frac{1}{N(x_n)} \frac{dN(x_n)}{dx_n}$$

FYI ONLY



- ▶ Sub doping profile $N(x_n)$ into $E(x_n)$:

$$N(x_n) = N(0)e^{-ax_n/W_b}$$

$$a = \ln \frac{N(0)}{N(W_b)}$$

$$E(x_n) = \frac{kT}{q} \frac{a}{W_b}$$

- ▶ Okay, so we derived it... tell me practically what caused this (think diffusion)...

.... Change in doping conc. vs. distance causes diffusion (from high conc. to low conc. or from left to right) this leaves (+ N_d) at left and excess (-e) at right, therefore built-in potential

- ▶ $E(x_n)$ is positive: therefore transit time (τ_t) for holes is decreased... this is important for high speed apps! **UIUC... >600 GHz HBT**

► Lets look at how the base width might change with V_{EC} ... (note V_{EB} , is forward biased). Lets look at how depletion width changes into the n-side (base)...

$$x_{n0} = \sqrt{\frac{2\epsilon V_0}{q} \frac{N_a}{N_d(N_a + N_d)}}$$

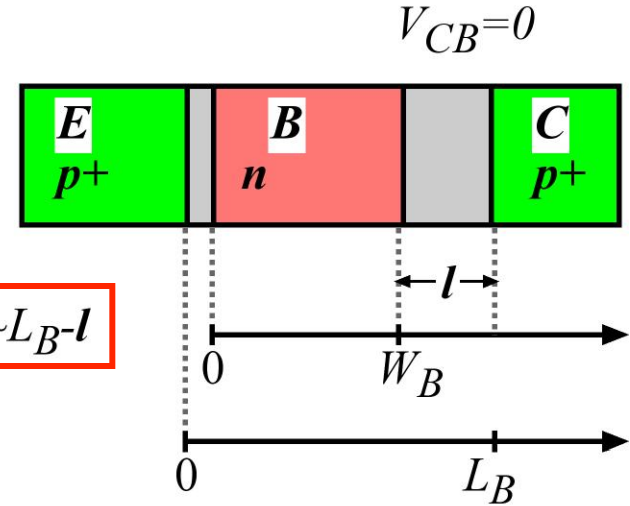
- 1) $V_0 + V_{BC} \sim -V_{BC}$
 2) for p^+np^+ $N_D \ll N_A$

$$x_{n0} = l = \sqrt{\frac{2\epsilon V_{BC}}{qN_d}}$$

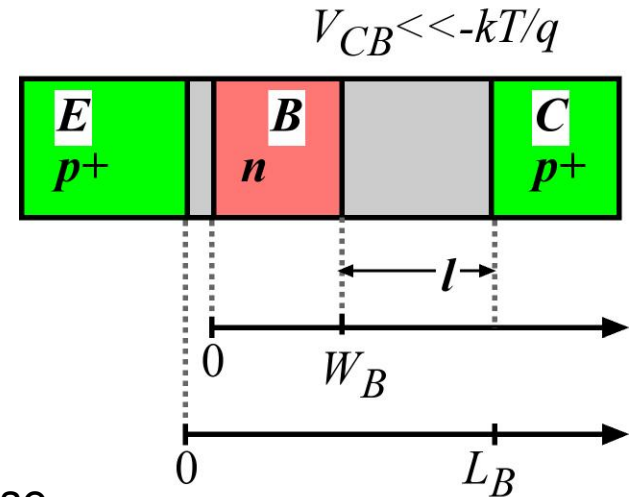
► We know if W_b decreases then the amplification factor β **increases**

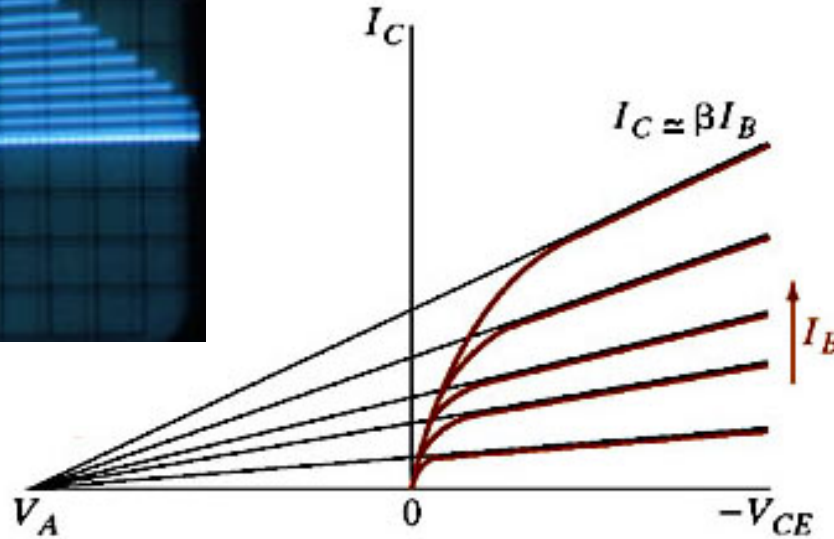
$$\frac{i_C}{i_B} = \frac{B\gamma}{1 - B\gamma} = \frac{\alpha}{1 - \alpha} = \beta = \text{sech} \frac{W_b}{L_p}$$

► If we increase V_{EC} (at fixed V_{EB}) then V_{BC} should increase ... so W_b should decrease, so β should increase... ☆



$$W_B \sim L_B - l$$





V_A = Early Voltage ★

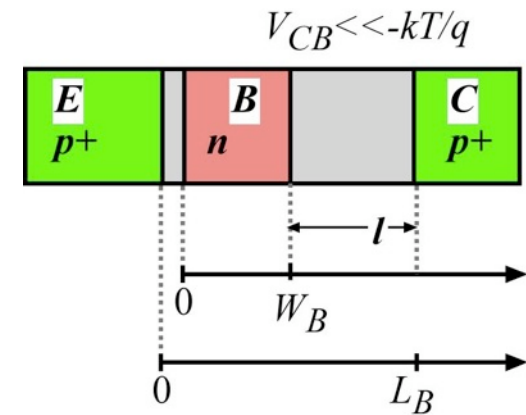
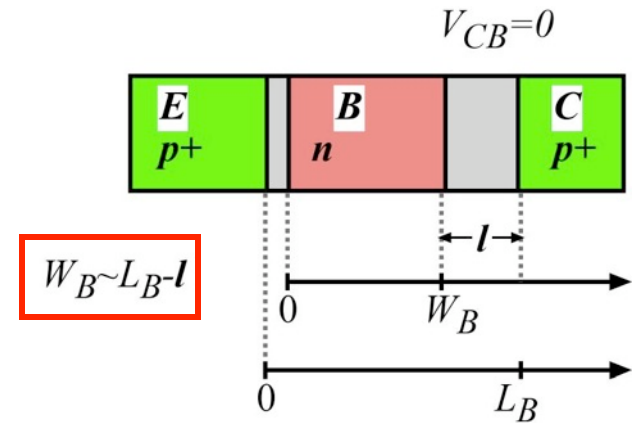
$$\frac{i_C}{i_B} = \frac{B\gamma}{1 - B\gamma} = \frac{\alpha}{1 - \alpha} = \beta = \text{sech} \frac{W_b}{L_p}$$

$$l = \sqrt{\frac{2\epsilon V_{BC}}{qN_d}}$$

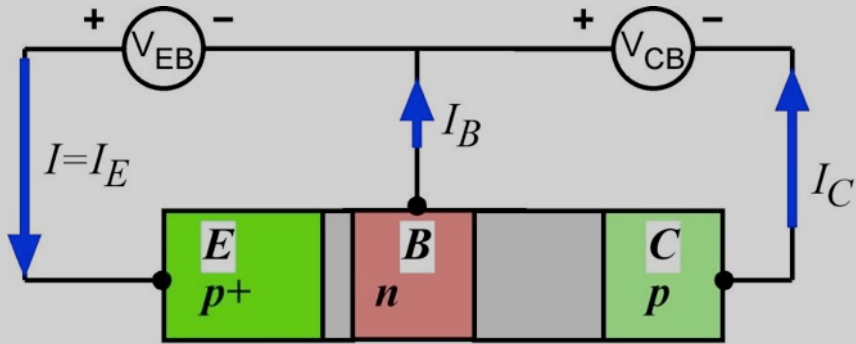
▶ If we increase V_{EC} (at fixed V_{EB}) then V_{BC} should increase ... so W_b should decrease, so β should increase...

▶ Large V_A implies weak base narrowing effect

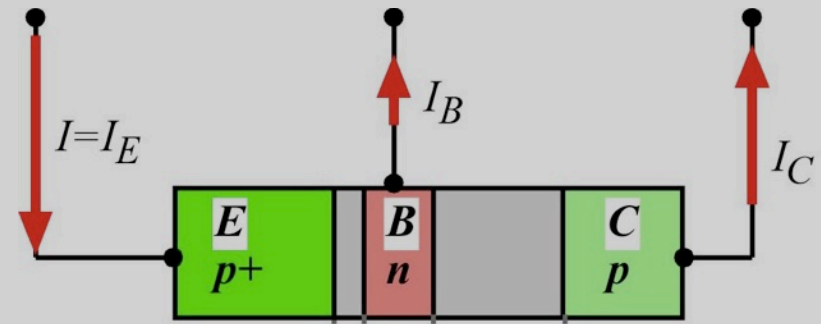
▶ Large V_A by graded doping... (what does this look like and why?, how do we achieve it during fabrication?)



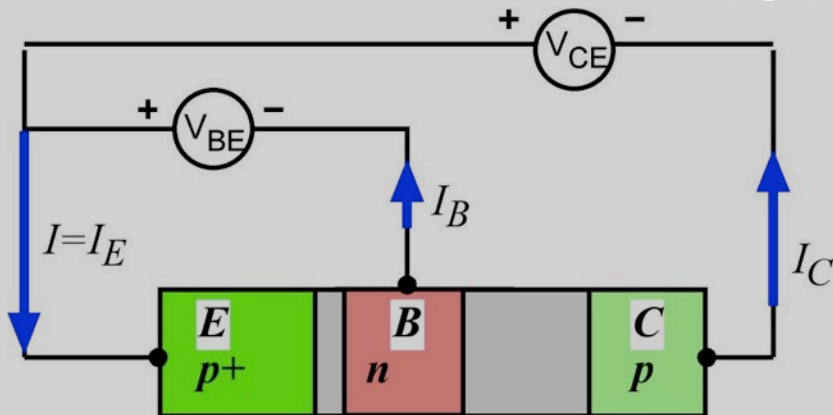
▶ Common Base (CB) configuration



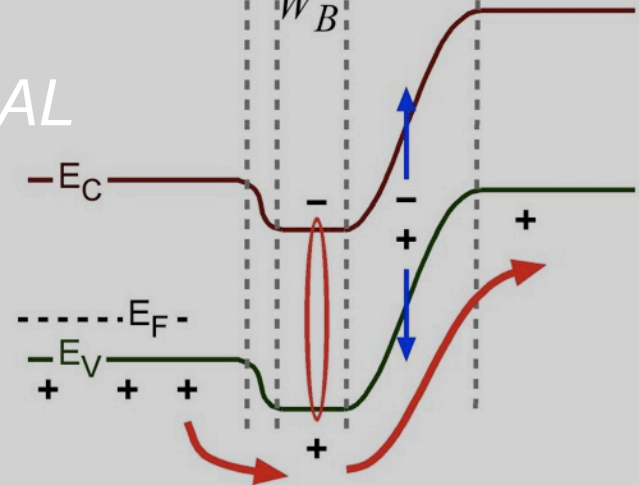
▶ Avalanche breakdown in BC increases I_C ...



▶ Common Emitter (CE) configuration



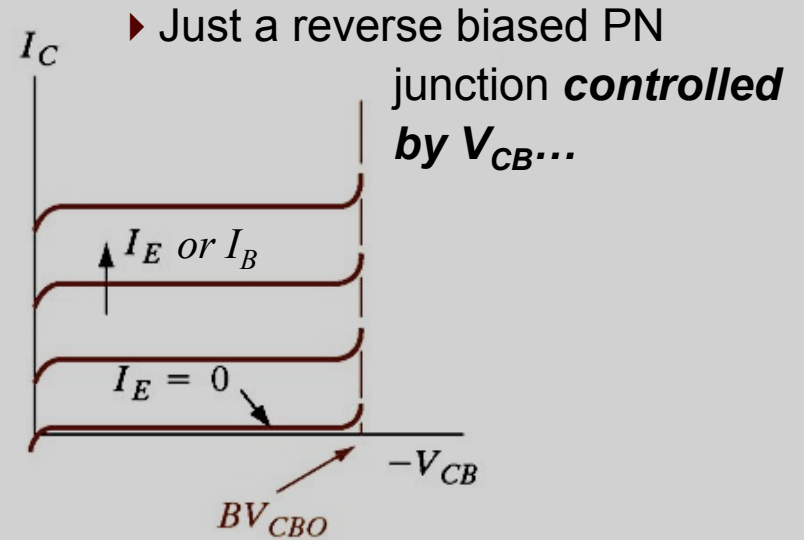
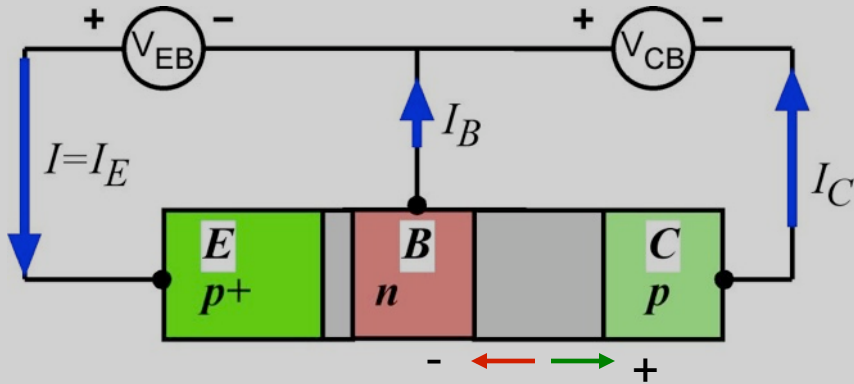
NOT CRITICAL



▶ However, onset of avalanche different for CB vs. the CE configurations!

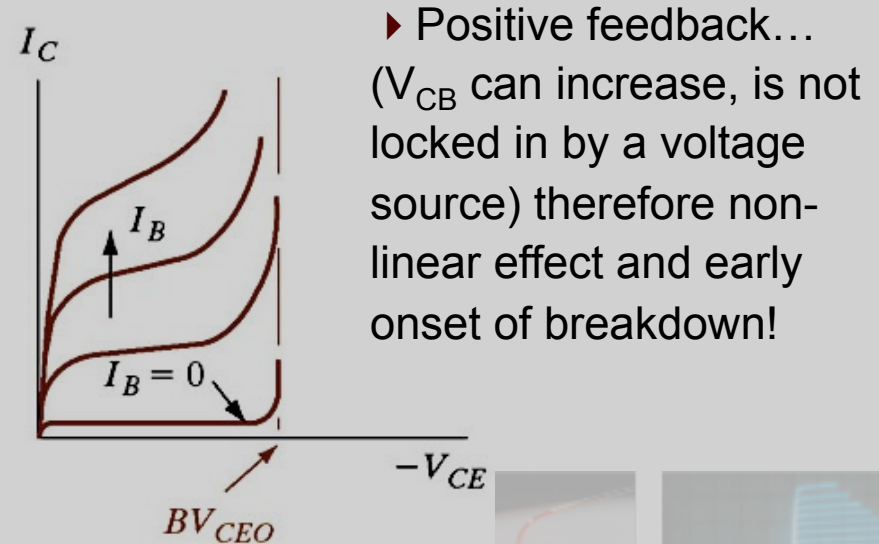
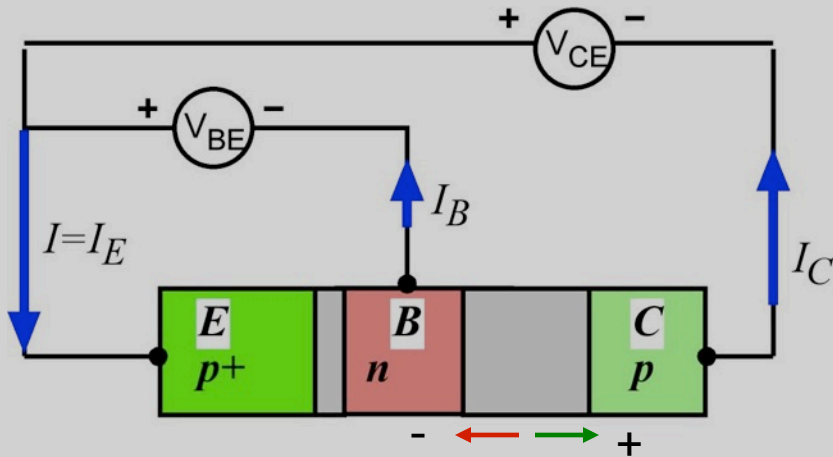


▶ Common Base (CB) configuration



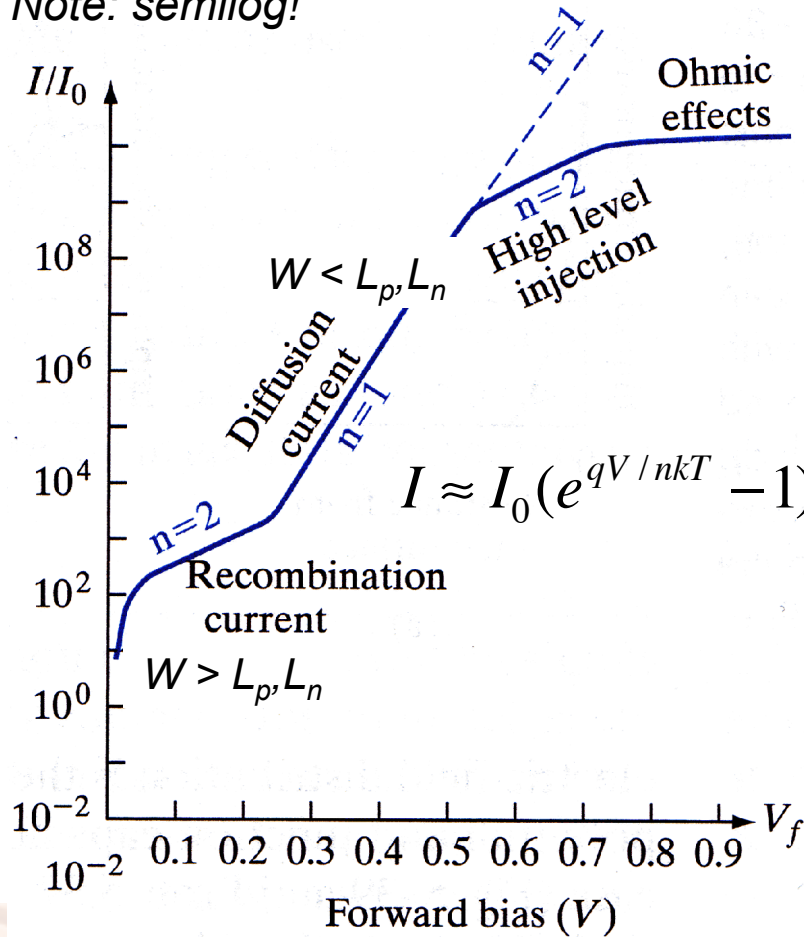
NOT CRITICAL

▶ Common Emitter (CE) configuration

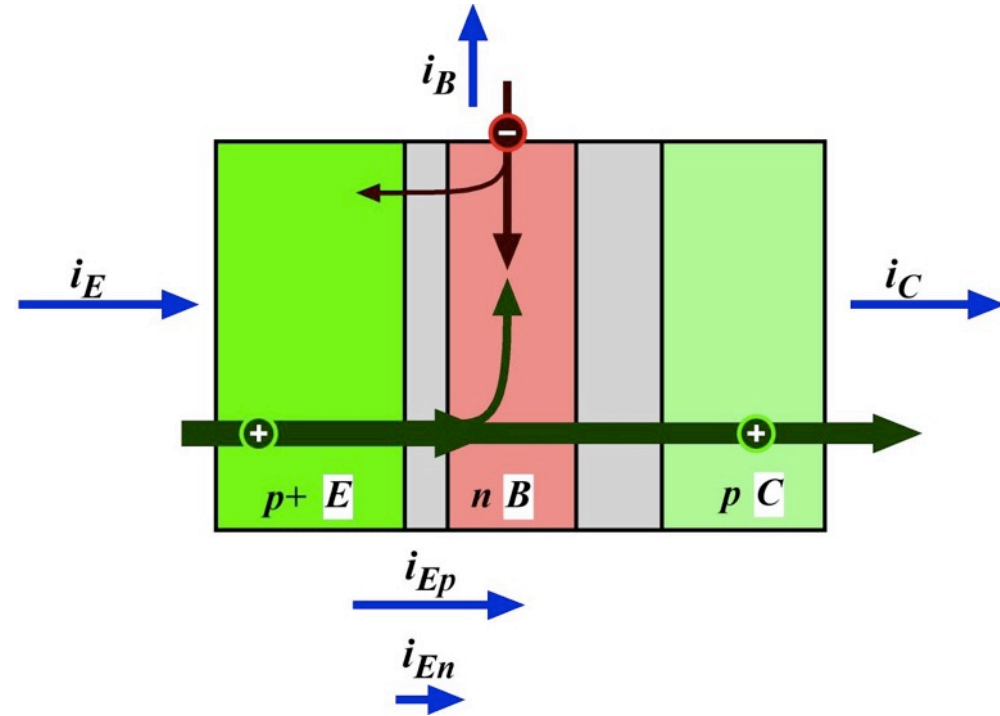


► Recall for the PN junction at low forward bias, the depletion region can be longer than L_p, L_n ... leading to recombination in the depletion region, reducing BJT performance. ☆

Note: semilog!

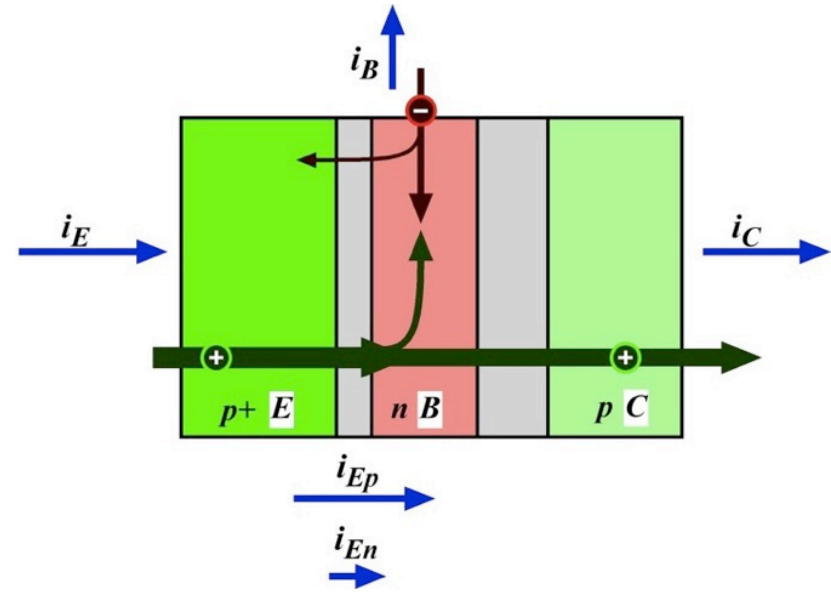


► For this effect, we care about the EB space charge region... but not the BC space charge region, why? ☆



$$\alpha = \frac{i_C}{i_E} = \frac{Bi_{Ep}}{i_{En} + i_{Ep}} = B\gamma \quad i_c = Bi_{Ep}$$

$$\gamma = i_{Ep} / (i_{En} + i_{Ep})$$



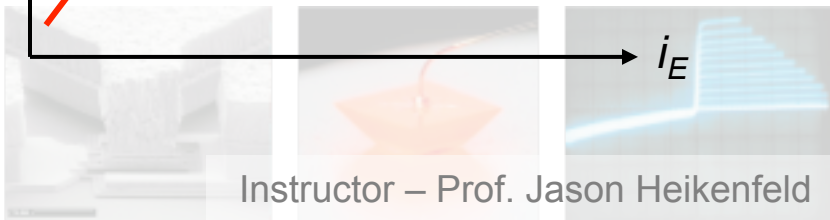
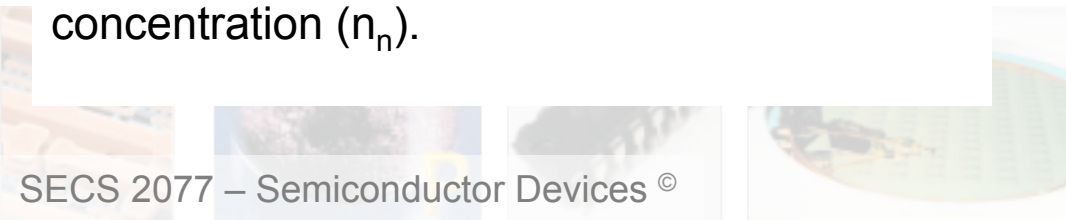
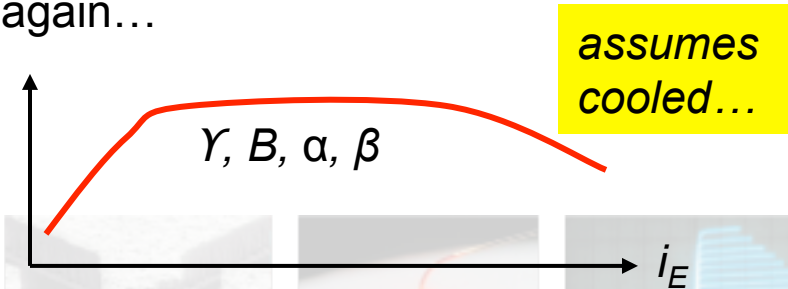
(1) At **low voltages**, some recombination occurs in the BE depletion region.

(2) At **moderate voltage** across EB γ, B, α, β reach normal values

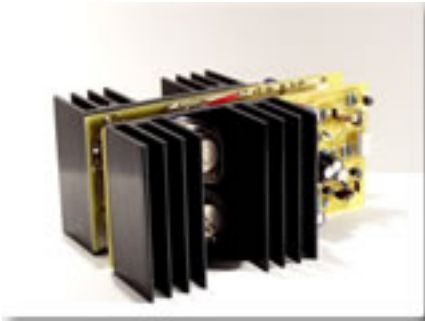
(3) At **higher voltages** (high injection levels) we can get so many holes (and therefore electrons, i_B) in the base that the excess electron concentration becomes significantly higher than the background electron concentration (n_n).

► This causes i_{En} to increase (looks more like p+n+ than p+n) and dec. γ as electrons spill into emitter. ☆

► And γ, B, α, β all start to decrease again...

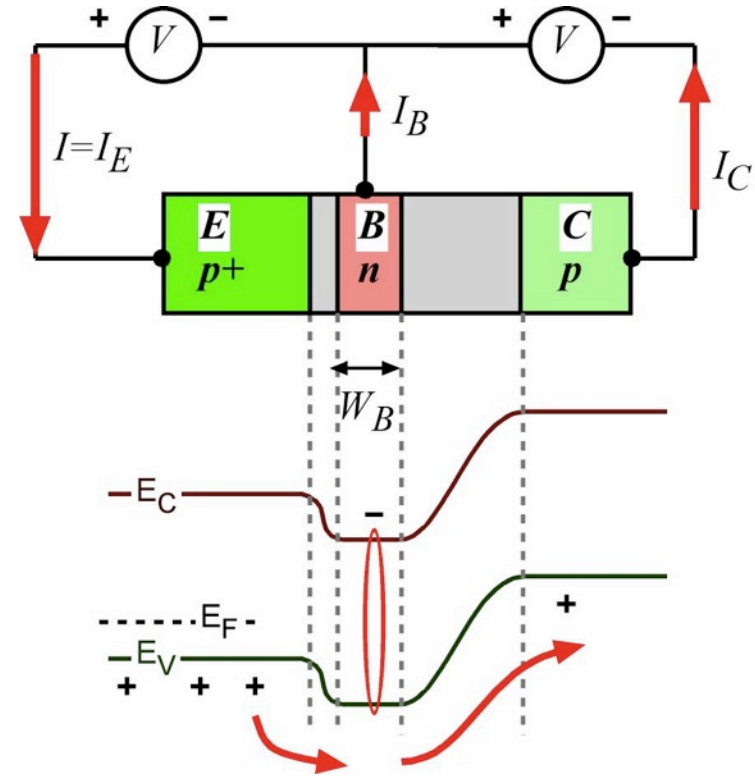


▶ These things must get hot...



▶ For example, at the collector junction $P=IV$... but how is the actual power dissipation happening? ☆

Answer: in base-collector depletion! Note the change in eV as holes go from base to collector... energy transferred to the lattice as vibrations (phonons)

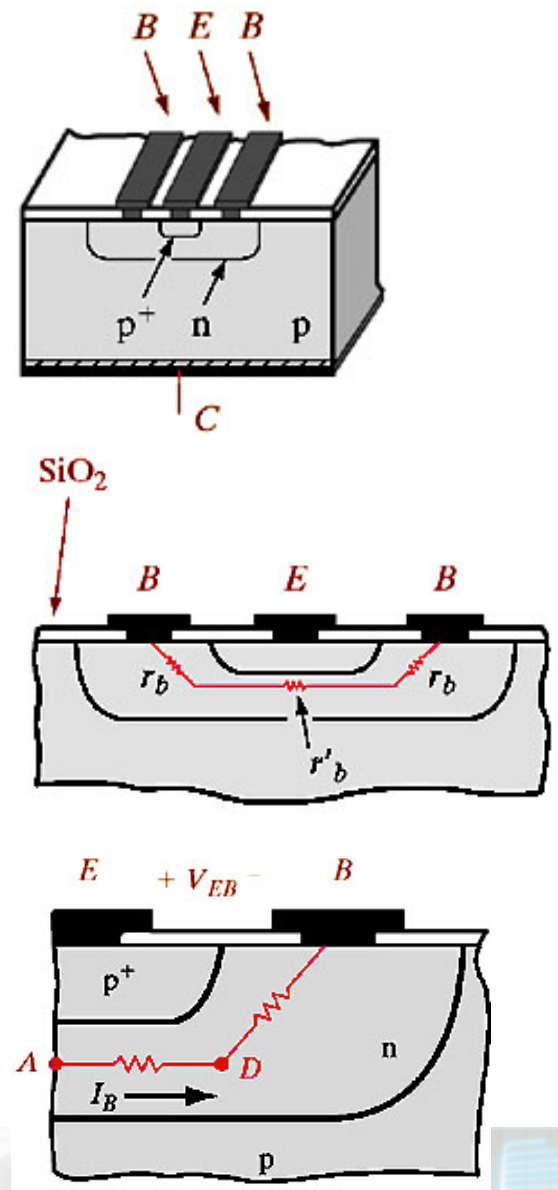


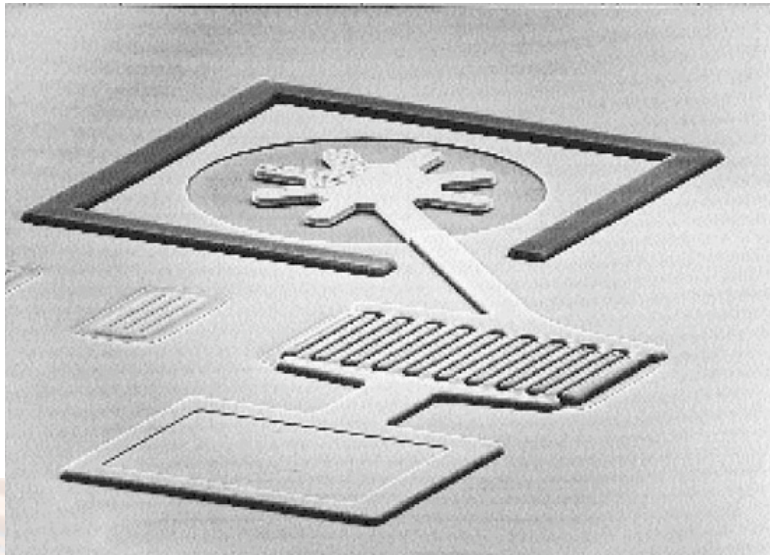
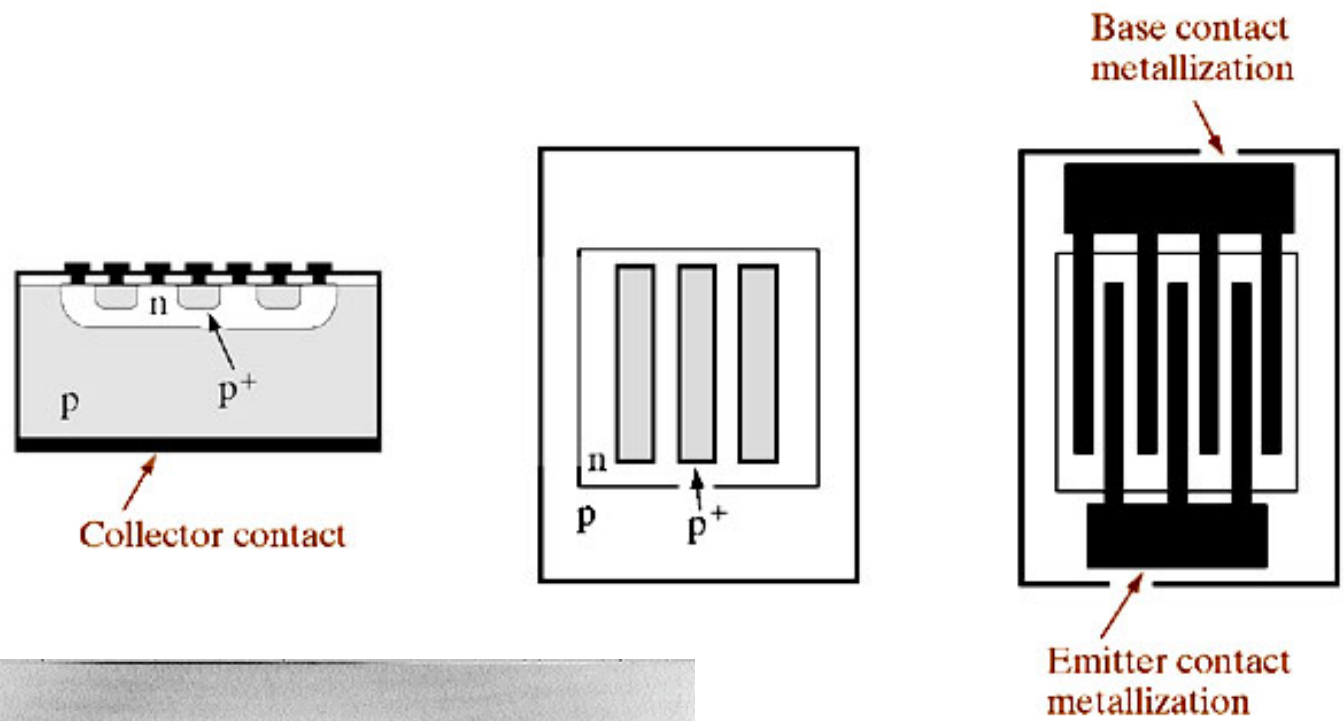
▶ Also... due to extrinsic recombination centers, τ_p in the base can actually increase with temperature... this causes gain to increase... causes more heat... causes more gain... etc.

▶ Therefore if not properly cooled ... thermal runaway (smoke)



- ▶ With conventional s/c the E and B are diffused in
- ▶ Since B is very lightly doped it is resistive and gets two contacts
- ▶ However, remember we want a thin base layer, and a large transistor area ($I_C = J_C * A$), so getting I_B under the center of the E is challenging
- ▶ This resistance causes larger V_{EB} at emitter edges and larger emitter current
- ▶ This ‘emitter current crowding’ causes heating (and we just established that effect can be problematic)



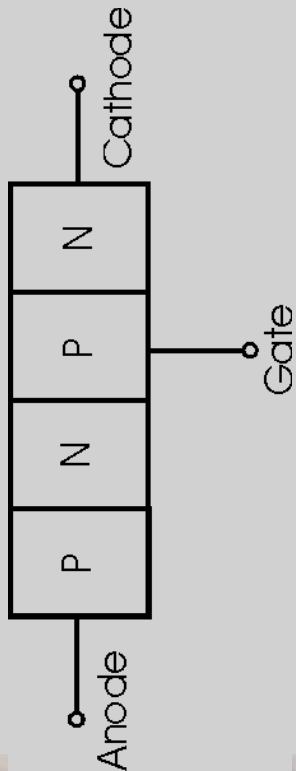


▶ A common solution to this is to still use a large area transistor but to interdigitate the emitter and base electrodes. ☆

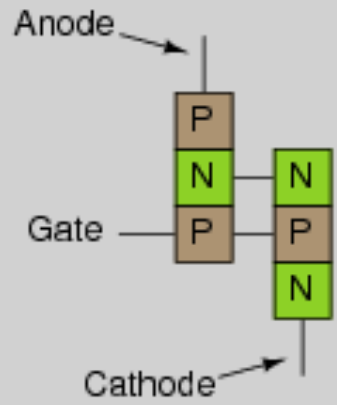
▶ So at left, where is our BJT?

▶ A common device is a silicon-controlled rectifier (SCR). It is beyond the scope of this course, but is basically two BJTs wired together! Classical lamp dimmers use these (and they are used in many other power sources as well).

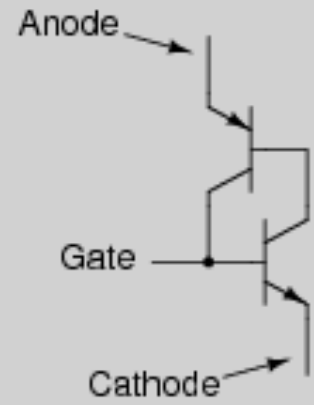
http://www.allaboutcircuits.com/vol_3/chpt_7/5.html



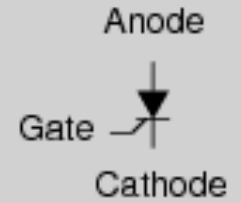
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Physical diagram



Equivalent schematic



Schematic symbol



▶ What is early voltage?

▶ In normal forward active mode, where is heat dissipated in the BJT? EB, BC, or everywhere?

▶ Why does BJT at right, perform worse at high I_C values?

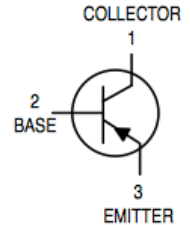
- (a) You run out of carriers to inject and the EB junction looks more like pn than p+n.
- (b) You inject more carriers than the doped concentration of the base, and the EB junction looks more like p+n+ than p+n.
- (c) The voltage is so high that breakdown starts to occur.
- (d) None of the above.

▶ To avoid current crowding, BJTs typically use:

- (a) Planar electrodes.
- (b) Interdigitated electrodes.
- (c) Current crowding cannot be avoided...

MOTOROLA SEMICONDUCTOR TECHNICAL DATA

Amplifier Transistor PNP Silicon



DC Current Gain

($I_C = -0.1$ mA dc, $V_{CE} = -10$ V dc)	75
($I_C = -1.0$ mA dc, $V_{CE} = -10$ V dc)	100
($I_C = -10$ mA dc, $V_{CE} = -10$ V dc)	100
($I_C = -150$ mA dc, $V_{CE} = -10$ V dc)(1)	100
($I_C = -500$ mA dc, $V_{CE} = -10$ V dc)(1)	50

